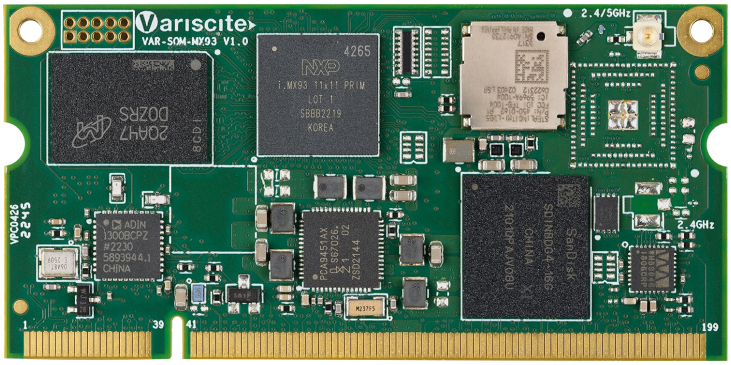
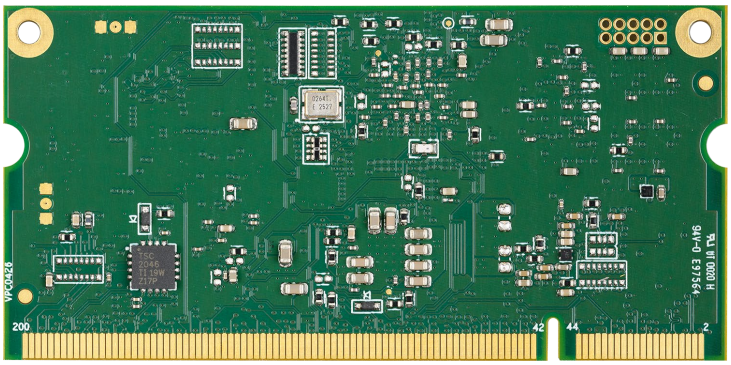
VARISCITE LTD.

VAR-SOM-MX93x V1.x Datasheet

NXP i.MX 93™ - based System-on-Module





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VAR-SOM-MX93 Datasheet

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1. Document Revision History

Revision	Date	Notes
1.0	October 21, 2022	Initial - Preliminary
1.1	January 22, 2023	Block diagram updated. Missing ground pins were added to the tables. Table 2, Pin 94 Note updated.
1.2	January 30, 2023	Block Diagram updated. eMMC size changed to maximum of 128GB. VBT assembly option added to Operating Voltages table.
1.3	February 13, 2023	Power Consumption values added. Storage Conditions added. Cosmetical changes.
1.4	February 23, 2023	Updated section 11

2. Table of Contents

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4. Overview

4.1 General Information

The VAR-SOM-MX93 offers a high-performance processing for a low-power System-on-Module. The product is based on the i.MX 93 family which represents NXP's latest power-optimized processors for smart home, building control, contactless HMI, IoT edge, and Industrial applications.

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency.

The VAR-SOM-MX93 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size, and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-MX93
  - ✓ Schematics
- VAR-DVK-MX93 full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-MX93
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP

Contact Variscite support services for further information: support@variscite.com.

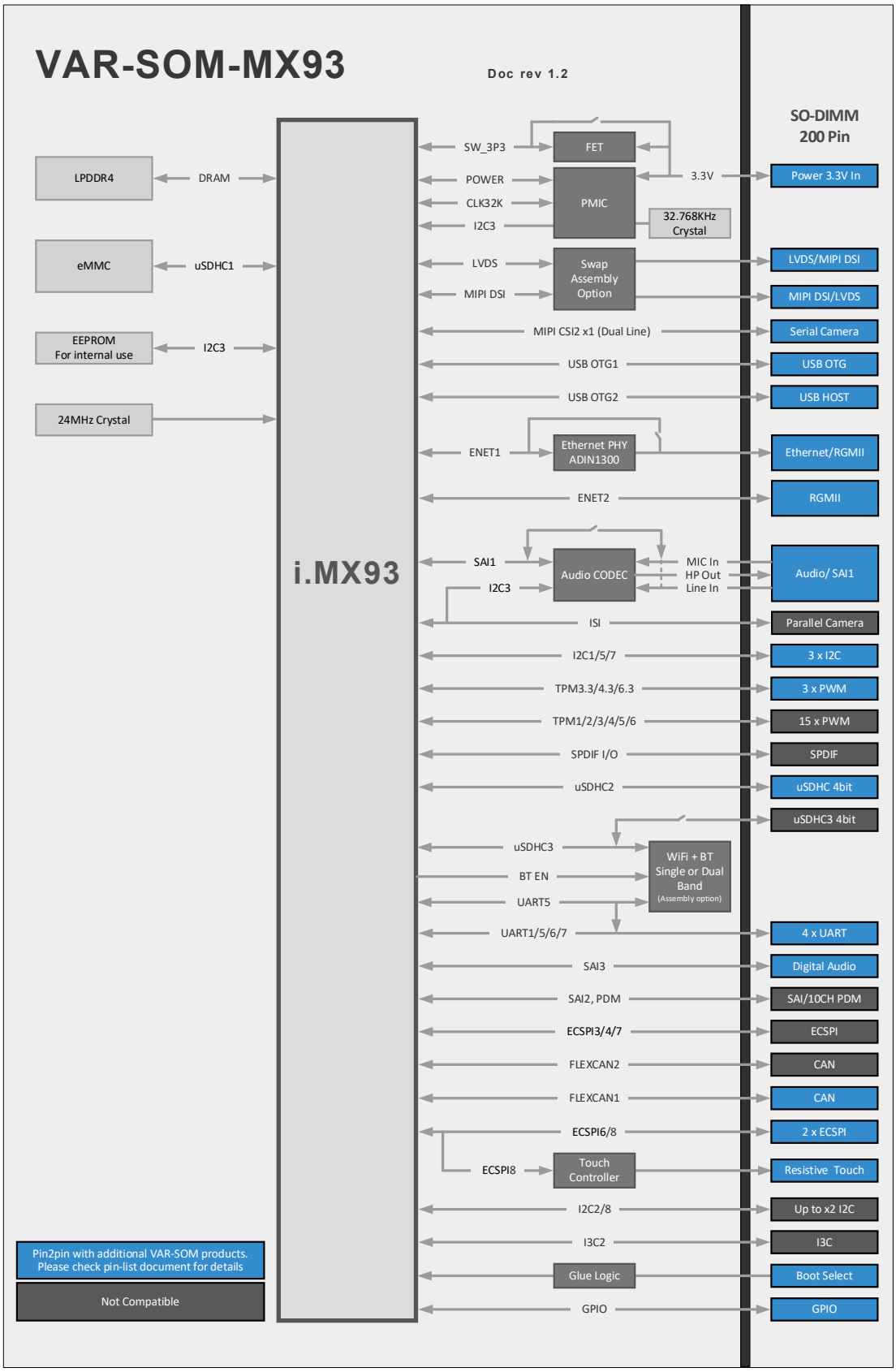
4.2 Feature Summary

- Cortex®-A55 MPCore platform
  - Two Cortex®-A55 processors operating up to 1.7 GHz
  - Media Processing Engine (MPE) with Arm® NEONTM technology supporting the Advanced Single Instruction Multiple Data architecture
  - Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
  - Support of 64-bit Arm® v8.2-A architecture
  - 256 KB cluster L3 cache
  - Parity/ECC protection on L1 cache, L2 cache, and TLB RAMs
- Cortex®-M33 core platform
  - Cortex®-M33 CPU operating up to 250 MHz
  - Support FPU
  - Support MPU
  - Support NVIC
  - Support FPB
  - Support DWT and ITM
  - Two-way set-associative 16 KB System Cache with parity support
  - Two-way set-associative 16 KB Code Cache with parity support
  - 256 KB tightly coupled memory (TCM)
- Neural Processing Unit (NPU)
  - Neural Network performance (256 MACs operating up to 1.0 GHz and 2 OPS/MAC)
  - NPU targets 8-bit and 16-bit integer RNN
  - Handles 8-bit weights
- Image Sensor Interface (ISI)
  - Standard pixel formats commonly used in many camera input protocols
  - Programmable resolutions up to 2K
  - Image processing for:
    - Supports one source of up to 2K horizontal resolution
    - Supports pixel rate up to 200 Mpixel/s
  - Image down scaling via decimation and bi-phase filtering
  - Color space conversion
  - Interlaced to progressive conversions
- On-chip memory
  - Boot ROM (256 KB) for Cortex®-A55
  - Boot ROM (256 KB) for Cortex®-M33
  - On-chip RAM (640 KB)
- RAM memory
  - Up to 2GBytes of LPDDR4/LPDDR4X RAM
- Storage
  - Up to 128GBytes of eMMC5.1 (8bit) interface supporting up to 400MB/sec
- Pixel Pipeline (PXP)
  - BitBlit
  - Flexible image composition options—alpha, chroma key
  - Porter-Duff operation
  - Image rotation (90o, 180o, 270o)
  - Image resize
  - Color space conversion
  - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
  - Standard 2D-DMA operation

- LCDIF Display Controller
  - The LCDIF can drive any of:
    - MIPI DSI: up to 1920x1200p60
    - LVDS Tx: up to 1366x768p60 or 1280x800p60
- MIPI CSI-2 Interface
  - One 2-lane MIPI CSI-2 camera input:
  - Complaint with MIPI CSI-2 specification v1.2 and MIPI D-PHY specification v1.2
  - Support up to 2 Rx data lanes (plus 1 Rx clock lane)
  - Support 80 Mbps – 1.5 Gbps per lane data rate in high-speed operation
  - Support 10 Mbps data rate in low power operation
- MIPI DSI Interface
  - One 4-lane MIPI DSI display with data supplied by the LCDIF
    - Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
    - Capable of resolutions achievable with a 200 MHz pixel clock and active pixel rate of 140 Mpixel/s with 24-bit RGB.
    - Support 80 Mbps—1.5 Gbps data rate per lane in high-speed operation
    - Support 10 Mbps data rate in low power operation
- Other Interfaces
  - SDIO/MMC
  - Resistive touch controller
  - Serial interfaces (ECSPI, FlexSPI, I2C, UART, CAN, JTAG, SAI)
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67.6 mm x 33 mm x 3.4 mm
- Industrial temperature range: -40°C to 85°C

4.3 Block Diagram

Figure 1 : VAR-SOM-MX93 Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX93.

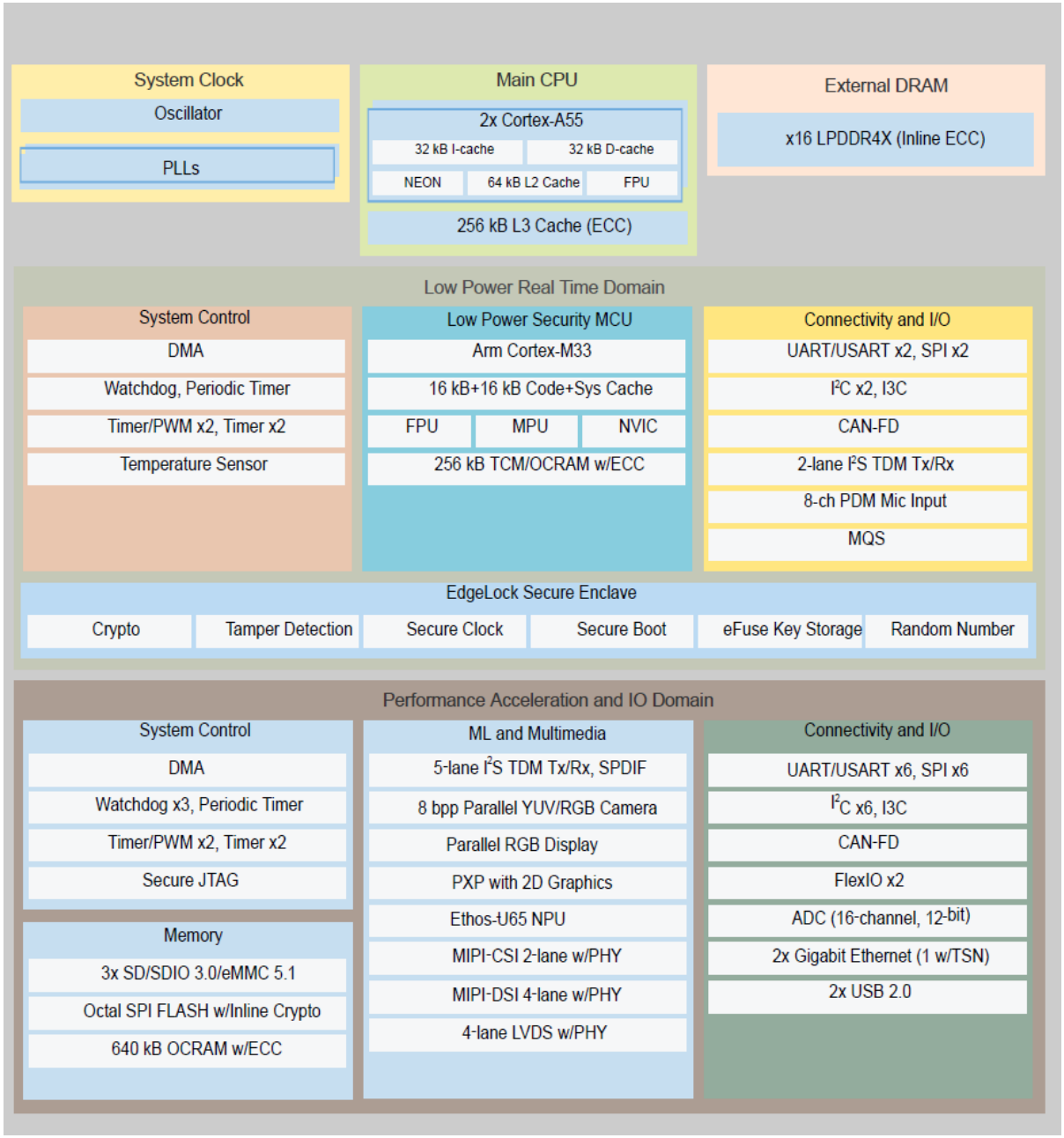
5.1 NXP i.MX 93

5.1.1 Overview

i. MX 93 applications processors deliver efficient machine learning (ML) acceleration and advanced security with integrated EdgeLock® secure enclave to support energy-efficient edge computing.
The i.MX 93 applications processors are the first in the i.MX portfolio to integrate the scalable Arm Cortex®-A55 core, bringing performance and energy efficiency to Linux®-based edge applications and the Arm Ethos®-U65 microNPU, enabling developers to create more capable, cost-effective, and energy-efficient ML applications.
Optimizing performance and power efficiency for Industrial, IoT and automotive devices, i.MX 93 processors are built with NXP's innovative Energy Flex architecture. The SoCs offer a rich set of peripherals targeting automotive, industrial and consumer IoT market segments.
Part of the EdgeVerse™ portfolio of intelligent edge solutions, the i.MX 93 family will be offered in commercial, industrial, extended industrial and automotive level qualification and backed by NXP's product longevity program.

5.1.2 i.MX93 Block Diagram

Figure 2 : i.MX93 Block Diagram



5.1.3 Arm Cortex®-A55 MPCore cluster

- One cluster of 2x Cortex-A55 cores
- Each core includes 32kB L1-I, 32kB L1-D and 64kB L2 cache per core
- 256kB shared cluster L3 cache
- Core cache protection (parity/ECC) supported

5.1.4 Arm Cortex®-M33 Platform

- Microcontroller available both for boot and for customer application
- Arm Cortex®-M33 Processor:
  - 16KB L1 Instruction Cache
  - 16KB L1 Data Cache
  - 256 KByte TCM, also accessible as SRAM by the rest of the system
- ECC support for both cache and TCM

5.1.5 On Chip Memory

- Boot ROM (256KB)
- 256KB Tightly Coupled RAM (TCM) for CM33, with ECC
- 640KB of SoC-specific OCRAM

5.1.6 External Memory

- One 16-bit DRAM controller:
  - Maximum supported capacity is 2GByte
  - LPDDR4X supported

5.1.7 Graphics

- PXP 2D accelerator
- LCDIF display
  - LDB and 4-lane LVDS display (up to 1366x768 or 1280x800)
  - Parallel display (up to 1366x768 or 1280x800)
  - One 4-lane MIPI-DPHY DSI Tx PHY and MIPI-DSI Controller
- ISI camera interface
  - MIPI-DPHY CSI Rx PHY and MIPI-CSI Controller compliant to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
  - Image processing for
    - One processed camera stream at 1080p30, or
    - One not processed camera stream (no scaling) at 4kp30 depending on system loading and use case
  - Image down scaling via decimation and bi-phase filtering
  - Color space conversion
  - Interlaced to progressive conversions

5.1.8 Machine Learning

- High-efficiency Neural-network Processing Unit (NPU)

5.1.9 Audio

- SPDIF supports raw capture mode that can save all the incoming bits into audio buffer.
- Up to 3x Synchronous Audio Interface (SAI) modules supporting I2S, AC97, TDM, and Codec/DSP interfaces
- Digital microphone input, up to 8-channel PDM

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.10 Connectivity

- 2x USB 2.0 OTG controller with integrated PHY interfaces
- 3x Ultra Secure Digital Host Controller (uSDHC) interfaces
    - uSDHC1 with boot support for eMMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
    - uSDHC2 with boot support for SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec
    - Support for SDXC (extended capacity)
    - USDHC3 to support use cases that need simultaneous support for all three of 1x eMMC, 1x SD Card and 1x SDIO (for WIFI connectivity)
- Up to 8x Universal asynchronous receiver/transmitter (LPUARTs) modules
- Up to 8x LPSPI modules
- Up to 8x I2C modules
- Up to 2x I3C modules
- Up to 2x CAN-FD modules
- Up to 2x 32-pin FlexIO modules
- Up to 1x 1G-bit Ethernet with AVB support (ENET)

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.11 Timers and PWMs

- 2x Low Power Periodical Interrupt Timer (LPIT)
  - 4 channels
  - 4 external trigger sources
  - Generic 32-bit resolution timer
  - Periodical interrupt generation
- 6x Timer/PWM module (TPM)
  - Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
  - 16-bit counter, support free-running counter or modulo counter mode, counting-up or down
  - Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center aligned PWM mode
- 2x Low-Power Timer (LPTMR)
- 5x WatchDog modules (WDOG)

Note: *The above list refers to the chip capabilities, part of the pins is used on the SOM therefore the exact number of interfaces can be lower.*

5.1.12 GPIO and Pin Multiplexing:

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.13 Analog:

- 1x 12-bit Analog Digital Converter (ADC)

5.1.14 Security:

- TRDC – Resource Domain Controller
  - Supports up to 16 resource domains
- Arm TrustZone® (TZ) architecture
- Secure and trusted access control
- Battery Backed Security Module (BBSM)
  - Monotonic counter - Secure real-time clock (RTC) - Zeroizable Master Key

5.1.15 System Debug

- Arm CoreSight® debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Support for 5-pin (JTAG) and SWD debug interfaces

5.1.16 Power Management

- One PMIC to supply all power rails.
- Temperature sensor with programmable trim points
- GPC hardware power management controller

5.2 Memory

5.2.1 RAM

The VAR-SOM-MX93 is available with up to 2GB of LPDDR4 or LPDDR4X memory.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-MX93 is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader, and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping, and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT

VAR-SOM-MX93 module can be configured either for Dual band or Single Band Wi-Fi® and Bluetooth® add on modules. Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

VAR-SOM-MX93 Wi-Fi and BT Key Features:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR, and BLE 5.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

5.4.1 VAR-SOM-MX93 Dual Band Option

The VAR-SOM-MX93 contains LSR's certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 5.2 wireless connectivity.

5.4.2 VAR-SOM-MX93 Single Band Option

The VAR-SOM-MX93 contains Laird's certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n,
BT 2.1+EDR, and BLE 5.2 wireless connectivity.

5.5 PMIC

The VAR-SOM-MX93 features Dual Freescale/NXP's PCA9541 chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 93 series of application processors. The PCA9541 regulates power rails required on SOM from a single 3.3V power supply.
The PMIC is fully programmable via the I2C interface and associated register map.
Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 10/100/1000 Mbps Ethernet Transceiver

The VAR-SOM-MX93 features on board an ADIN1300 Integrated Ethernet Transceiver.
Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Auto-negotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 Resistive Touch Controller (TSC2046)

The VAR-SOM-MX93 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

5.8 EEPROM

The VAR-SOM-MX93 uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters. This EEPROM is connected to I2C3 bus and intended only for holding the above information. The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-MX93 Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-MX93.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	Dual band Wi-Fi and BT/BLE combo assembled on SOM
WB	Single band Wi-Fi and BT/BLE combo assembled on SOM
TP	Resistive Touch controller assembled on SOM
DSCM	DSI and LVDS0 lanes are swapped to allow pin to pin compatibility to VAR-SOM-MX8M family when DSI interface is used.
VBT	Power supply supports battery voltage levels 3.3V – 5.5V

Note: *Other orderable options are available and are not part of this datasheet.*
Please refer to Variscite official website for full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-MX93 exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi “WB” or “WBD” Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 VAR-SOM-MX93 Connector Pin-out

Table 2: VAR-SOM-MX93 J1 Pinout

Pin	Assembly	Pin name	Notes	GPIO	Ball
1	No EC	ENET1_TX_CTL	1.8V level signal	GPIO4.IO[6]	V10
1	EC	NC			
2		GND			
3	No EC	ENET1_TD3	1.8V level signal	GPIO4.IO[2]	V12
3	EC	ETH0_MDI_A_P			ADIN1300BCPZ.12
4	No EC	ENET1_RD0	1.8V level signal	GPIO4.IO[10]	AA8
4	EC	ETH0_MDI_C_P			ADIN1300BCPZ.16
5	No EC	ENET1_TD2	1.8V level signal	GPIO4.IO[3]	U12
5	EC	ETH0_MDI_A_M			ADIN1300BCPZ.13
6	No EC	ENET1_RD1	1.8V level signal	GPIO4.IO[11]	Y9
6	EC	ETH0_MDI_C_M			ADIN1300BCPZ.17
7		GND			
8		GND			
9	No EC	ENET1_TD1	1.8V level signal	GPIO4.IO[4]	T12
9	EC	ETH0_MDI_B_P			ADIN1300BCPZ.14
10	No EC	ENET1_RD2	1.8V level signal	GPIO4.IO[12]	AA9
10	EC	ETH0_MDI_D_P			ADIN1300BCPZ.18
11	No EC	ENET1_TD0	1.8V level signal	GPIO4.IO[5]	W11
11	EC	ETH0_MDI_B_M			ADIN1300BCPZ.15
12	No EC	ENET1_RD3	1.8V level signal	GPIO4.IO[13]	Y10
12	EC	ETH0_MDI_D_M			ADIN1300BCPZ.19
13		GND			
14		GND			
15	No EC	ENET1_RX_CTL	1.8V level signal	GPIO4.IO[8]	Y8
15	EC	ETH0_LED_ACT	Has on SOM 10K pull up		ADIN1300BCPZ.21
16	No EC	ENET1_RXC	1.8V level signal	GPIO4.IO[9]	AA7
16	EC	ETH0_LED_LINK	Has on SOM open drain inverter		ADIN1300BCPZ.26
17		GPIO_IO24		GPIO2.IO[24]	U21
18	No AC	SAI1_TXD0		GPIO1.IO[13]	H21
18	AC	DMIC_CLK			WM8904CGEFL.1
19		GND			
20	No AC	UART2_RXD		GPIO1.IO[6]	F20
20	AC	DMIC_DATA	Has on SOM voltage divider		WM8904CGEFL.27
21		GPIO_IO20		GPIO2.IO[20]	T20
22		GPIO_IO18		GPIO2.IO[18]	R18
23		GPIO_IO19		GPIO2.IO[19]	R17
24		GPIO_IO26		GPIO2.IO[26]	V20
25		GPIO_IO16		GPIO2.IO[16]	R21

Pin	Assembly	Pin name	Notes	GPIO	Ball
26		GPIO_IO21		GPIO2.IO[21]	T21
27		GND			
28		GND			
29		CCM_CLKO1	1.8V level signal. Has an internal 12K pull down	GPIO3.IO[26]	AA2
30		ENET1_MDIO	Goes through level translator Pin function cannot be altered on EC type SOMs	GPIO4.IO[1]	AA10
31	No WB No WBD	SD3_DATA1		GPIO3.IO[23]	V14
31	WB	NC			
31	WBD	NC			
32		VBAT			
33	No WB No WBD	SD3_DATA2		GPIO3.IO[24]	U14
33	WB	NC			
33	WBD	NC			
34		VBAT			
35	No WB No WBD	SD3_DATA3		GPIO3.IO[25]	T14
35	WB	NC			
35	WBD	NC			
36		NC			
37		GND			
38		NC			
39		GPIO_IO00	Cannot be configured as I2C3	GPIO2.IO[0]	J21
40		CCM_CLKO2	1.8V level signal	GPIO3.IO[27]	Y3
41		GPIO_IO01	Cannot be configured as I2C3	GPIO2.IO[1]	J20
42		BOOT_SEL			
43		GPIO_IO03		GPIO2.IO[3]	K21
44		PDM_CLK		GPIO1.IO[8]	G17
45		GPIO_IO02		GPIO2.IO[2]	K20
46		PDM_BIT_STREAM0		GPIO1.IO[9]	J17
47		GND			
48		GPIO_IO10		GPIO2.IO[10]	N17
49		SOM_3V3_PER			
50		DAP_TMS_SWDIO	1.8V level signal. Can be used if BT disabled. Has an internal 10K pull down	GPIO3.IO[29]	W2
51		DAP_TCLK_SWCLK	1.8V level signal. Can be used if BT disabled.	GPIO3.IO[30]	Y1
52		DAP_TDO_TRACES WO	1.8V level signal. Can be used if BT disabled.	GPIO3.IO[31]	Y2
53		DAP_TDI	1.8V level signal. Can be used if BT disabled.	GPIO3.IO[28]	W1
54		ENET2_RD3	1.8V level signal	GPIO4.IO[27]	Y6
55		ENET2_TD3	1.8V level signal	GPIO4.IO[16]	T10
56		ENET2_TD2	1.8V level signal	GPIO4.IO[17]	V8

Pin	Assembly	Pin name	Notes	GPIO	Ball
57		ENET2_RXC	1.8V level signal	GPIO4.IO[23]	AA3
58	No EC	ENET1_TXC	1.8V level signal	GPIO4.IO[7]	U10
58	EC	NC			
59		GND			
60		SD2_CLK	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[1]	AA19
61		SD2_DATA2	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[5]	Y20
62		SD2_DATA0	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[3]	Y18
63		SD2_DATA1	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[4]	AA18
64		SD2_CMD	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[2]	Y19
65		SD2_DATA3	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[6]	AA20
66		GND			
67		GND			
68		GPIO_IO25		GPIO2.IO[25]	V21
69		GPIO_IO27		GPIO2.IO[27]	W21
70		NC			
71		ENET2_RD2	1.8V level signal	GPIO4.IO[26]	AA5
72		PDM_BIT_STREAM1		GPIO1.IO[10]	G18
73		ENET2_TD0	1.8V level signal	GPIO4.IO[19]	T8
74		ENET1_MDC	Goes through level translator Pin function cannot be altered on EC type SOMs	GPIO4.IO[0]	AA11
75		CCM_CLKO3	1.8V level signal	GPIO4.IO[28]	U4
76		GND			
77		GPIO_IO11		GPIO2.IO[11]	N18
78		GND			
79		NC			
80		SD2_CD_B	Can be 3.3V or 1.8V depending on SD Card type	GPIO3.IO[0]	Y17
81		ENET2_RD1	1.8V level signal	GPIO4.IO[25]	Y5
82		NC			
83		UART1_RXD		GPIO1.IO[4]	E20
84	No WB No WBD	SD3_DATA0		GPIO3.IO[22]	T16
84	WB	NC			
84	WBD	NC			
85		UART1_TXD		GPIO1.IO[5]	E21
86		GPIO_IO17		GPIO2.IO[17]	R20
87		GPIO_IO22		GPIO2.IO[22]	U18
88		GPIO_IO23		GPIO2.IO[23]	U20
89		GND			
90		I2C1_SDA		GPIO1.IO[1]	C21
91		BT_PCM_CLK	1.8V level signal		450-01159R.55, 450-0162R.42
92		I2C1_SCL		GPIO1.IO[0]	C20
93		BT_PCM_IN	1.8V level signal		450-01159R.146, 450-0162R.41

Pin	Assembly	Pin name	Notes	GPIO	Ball
94		USB1_ID	1.8V level signal		C11
95		GND			
96		ENET2_TXC	1.8V level signal	GPIO4.IO[21]	U6
97		BT_PCM_OUT	1.8V level signal		450-01159R.145, 450-0162R.44
98		SYS_NRST	Open drain. Has an internal 100k pull up		
99		BT_PCM_SYNC	1.8V level signal		450-01159R.144, 450-0162R.43
100		NC			
101		GND			
102		NC			
103		VBAT			
104		USB2_VBUS	5V level		E14
105		VBAT			
106		USB1_VBUS	5V level		F12
107		VBAT			
108		USB2_D_N			A15
109		VBAT			
110		USB2_D_P			B15
111		VBAT			
112		GND			
113		ENET2_TX_CTL	1.8V level signal	GPIO4.IO[20]	V6
114		USB1_D_N			A14
115		GPIO_IO05		GPIO2.IO[5]	L18
116		USB1_D_P			B14
117		NC			
118		GND			
119		MIPI_CSI1_D0_P			B11
120		ENET2_RX_CTL	1.8V level signal	GPIO4.IO[22]	Y4
121		MIPI_CSI1_D0_N			A11
122		ENET2_RD0	1.8V level signal	GPIO4.IO[24]	AA4
123		MIPI_CSI1_D1_N			A10
124		GPIO_IO08		GPIO2.IO[8]	M20
125		MIPI_CSI1_D1_P			B10
126		GND			
127		NC			
128		WIFI_HOST_WAKE	1.8V level signal		450-01159R.131, 450-0162R.17
129		NC			
130		BT_DEV_WAKE	1.8V level signal		450-01159R.56, 450-0162R.47
131		WDOG_ANY	Used internally for RESET. Has an internal 100k Pull up	GPIO1.IO[15]	J18
132		GND			

Pin	Assembly	Pin name	Notes	GPIO	Ball
133		NC			
134		BT_HOST_WAKE	1.8V level signal		450-01159R.57, 450-0162R.46
135		MIPI_CSI1_CLK_P			E10
136		PMIC_NINT	1.8V level signal. No internal pull up.		PCA9451.13
137		MIPI_CSI1_CLK_N			D10
138		GND			
139		GND			
140		PMIC_STBY_REQ	1.8V level signal. Has an internal 100k Pull down.		B18
141		ETH_INT_1V8	1.8V level signal		ADIN1300.22
142		PMIC_ON_REQ	1.8V level signal. Has an internal 100k Pull down.		A17
143		ONOFF	1.8V level signal. Has an internal 100k Pull up.		A19
144		GND			
145	No WB No WBD	SD3_CLK		GPIO3.IO[20]	V16
145	WB	NC			
145	WBD	NC			
146		ADC_IN0	1.8V level signal		B19
147	No WB No WBD	SD3_CMD		GPIO3.IO[21]	U16
147	WB	NC			
147	WBD	NC			
148		ADC_IN1	1.8V level signal		A20
149		GND			
150		ADC_IN2	1.8V level signal		B20
151		ADC_IN3	1.8V level signal		B21
152		CLKIN1	1.8V level signal. Has an internal 100k Pull down.		B17
153		CLKIN2	1.8V level signal. Has an internal 100k Pull down.		A18
154		TAMPER0	1.8V level signal		B16
155		NC			
156		TAMPER1	1.8V level signal		F14
157		NC			
158		GND			
159		GND			
160	No DSCM	LVDS_D1_N			A4
160	DSCM	MIPI_DSI1_D1_N			A7
161	No DSCM	LVDS_D0_N			A5
161	DSCM	MIPI_DSI1_D0_N			A6
162	No DSCM	LVDS_D1_P			B4
162	DSCM	MIPI_DSI1_D1_P			B7

Pin	Assembly	Pin name	Notes	GPIO	Ball
163	No DSCM	LVDS_D0_P			B5
163	DSCM	MIPI_DSI1_D0_P			B6
164	No DSCM	LVDS_D2_N			A2
164	DSCM	MIPI_DSI1_D2_N			A8
165	No DSCM	LVDS_D3_N			B1
165	DSCM	MIPI_DSI1_D3_N			A9
166	No DSCM	LVDS_D2_P			B2
166	DSCM	MIPI_DSI1_D2_P			B8
167	No DSCM	LVDS_D3_P			C1
167	DSCM	MIPI_DSI1_D3_P			B9
168	No DSCM	LVDS_CLK_N			A3
168	DSCM	MIPI_DSI1_CLK_N			D6
169		GND			
170	No DSCM	LVDS_CLK_P			B3
170	DSCM	MIPI_DSI1_CLK_P			E6
171		GPIO_IO04		GPIO2.IO[4]	L17
172		GND			
173		NC			
174		GPIO_IO07		GPIO2.IO[7]	L21
175		GPIO_IO09		GPIO2.IO[9]	M21
176		GPIO_IO06		GPIO2.IO[6]	L20
177		ENET2_TD1	1.8V level signal	GPIO4.IO[18]	U8
178		GND			
179		GND			
180	No DSCM	MIPI_DSI1_CLK_N			D6
180	DSCM	LVDS_CLK_N			A3
181	No DSCM	MIPI_DSI1_D3_P			B9
181	DSCM	LVDS_D3_P			C1
182	No DSCM	MIPI_DSI1_CLK_P			E6
182	DSCM	LVDS_CLK_P			B3
183	No DSCM	MIPI_DSI1_D3_N			A9
183	DSCM	LVDS_D3_N			B1
184	No DSCM	MIPI_DSI1_D0_N			A6
184	DSCM	LVDS_D0_N			A5
185		GND			
186	No DSCM	MIPI_DSI1_D0_P			B6
186	DSCM	LVDS_D0_P			B5
187	No TP	GPIO_IO14		GPIO2.IO[14]	P20
187	TP	TS_X-			TSC2046IRGV.8
188	No DSCM	MIPI_DSI1_D1_N			A7
188	DSCM	LVDS_D1_N			A4

Pin	Assembly	Pin name	Notes	GPIO	Ball
189	No TP	GPIO_IO15		GPIO2.IO[15]	P21
189	TP	TS_X+			TSC2046IRGV.6
190	No DSCM	MIPI_DSI1_D1_P			B7
190	DSCM	LVDS_D1_P			B4
191	No TP	GPIO_IO12		GPIO2.IO[12]	N20
191	TP	TS_Y+			TSC2046IRGV.7
192	No DSCM	MIPI_DSI1_D2_N			A8
192	DSCM	LVDS_D2_N			A2
193	No TP	GPIO_IO13		GPIO2.IO[13]	N21
193	TP	TS_Y-			TSC2046IRGV.9
194	No DSCM	MIPI_DSI1_D2_P			B8
194	DSCM	LVDS_D2_P			B2
195		AGND			
196	No AC	I2C2_SCL		GPIO1.IO[2]	D20
196	AC	HPOUTFB			WM8904CGEFL.14
197	No AC	I2C2_SDA		GPIO1.IO[3]	D21
197	AC	LINEIN1_LP			WM8904CGEFL.26
198	No AC	SAI1_RXD0		GPIO1.IO[14]	H20
198	AC	HPLOUT	Includes on SOM audio filter		WM8904CGEFL.13
199	No AC	SAI1_TXFS		GPIO1.IO[11]	G21
199	AC	LINEIN1_RP			WM8904CGEFL.24
200	No AC	SAI1_TXC		GPIO1.IO[12]	G20
200	AC	HPROUT	Includes on SOM audio filter		WM8904CGEFL.15

7.4 VAR-SOM-MX93 Connector Pin Mux

Table 3: VAR-SOM-MX93 PINMUX

Pin	Assembly	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	No EC	enet_qos.RGMII_TX_CTL	uart3.DTR_B			flexio2.FLEXIO[6]	gpio4.IO[6]		
3	No EC	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]		
4	No EC	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]		
5	No EC	enet_qos.RGMII_TD2	INPUT=enet_qos.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]		
6	No EC	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]		
9	No EC	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B	
10	No EC	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]		
11	No EC	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]		
12	No EC	enet_qos.RGMII_RD3			lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]		
15	No EC	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]		
16	No EC	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]		
17		gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
18	No AC	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]		
20	No AC	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
21		gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]
22		gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]
23		gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
24		gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
25		gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]

Pin	Assembly	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
26		gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK
29		ccmsrcgpcmix.CLKO1				flexio1.FLEXIO[26]	gpio3.IO[26]		
30		enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]		
31	No WB or WBD	usdhc3.DATA1	flexspi.A_DATA[1]			flexio1.FLEXIO[23]	gpio3.IO[23]		
33	No WB or WBD	usdhc3.DATA2	flexspi.A_DATA[2]			flexio1.FLEXIO[24]	gpio3.IO[24]		
35	No WB or WBD	usdhc3.DATA3	flexspi.A_DATA[3]			flexio1.FLEXIO[25]	gpio3.IO[25]		
39		gpio2.IO[0]		isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
40		ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]		
41		gpio2.IO[1]		isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
43		gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
44		pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX	
45		gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
46		pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX	
48		gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
50		dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B	
51		dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B	
52		dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX	
53		dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX	
54		enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]		
55		enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]		
56		enet2.RGMII_TD2	INPUT=enet2.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]		
57		enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]		

Pin	Assembly	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
58	No EC	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]		
60		usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]		
61		usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
62		usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]		
63		usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		
64		usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]		
65		usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]		
68		gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
69		gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
71		enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]		
72		pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT3	gpio1.IO[10]		
73		enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]		
74		enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]		
75		ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]		
77		gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
80		usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
81		enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]		
83		uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]		
84	No WB or WBD	usdhc3.DATA0	flexspi.A_DATA[0]			flexio1.FLEXIO[22]	gpio3.IO[22]		
85		uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]		
86		gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
87		gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
88		gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]

Pin	Assembly	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
90		i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]		
92		i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]		
96		enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]		
113		enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]		
115		gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
120		enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]		
122		enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]		
124		gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
131		wdog1.WDOG_ANY							
140		bbsmmix.PMIC_STBY_REQ							
142		bbsmmix.PMIC_ON_REQ							
143		bbsmmix.ONOFF							
145	No WB or WBD	usdhc3.CLK	flexspi.A_SCLK			flexio1.FLEXIO[20]	gpio3.IO[20]		
146		anamix.adc_in0							
147	No WB or WBD	usdhc3.CMD	flexspi.A_SS0_B			flexio1.FLEXIO[21]	gpio3.IO[21]		
148		anamix.adc_in1							
150		anamix.adc_in2							
151		anamix.adc_in3							
152		anamix.CLKIN1	anamix.esd_diode						
153		anamix.CLKIN2	anamix.atx						
154		bbsmmix.TAMPER0							
156		bbsmmix.TAMPER1							
171		gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]

Pin	Assembly	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
174		gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]
175		gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]
176		gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
177		enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]		
187	TP	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]
189	TP	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
191	TP	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
193	TP	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
196	No AC	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
197	No AC	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
198	No AC	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
199	No AC	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]		
200	No AC	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI (CSI and DSI), LVDS	100 Ω Differential

8.2 Display Interfaces

The i.MX 93 SoC includes one instance of LCDIF
One LCDIF can drive any of three displays or drive the same output to multiple displays:

- MIPI DSI (up to 1920x1200p60)
- LVDS Tx (up to 1366x768p60 or 1280x800p60)
- Parallel Display

8.2.1 LVDS

The LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of
synchronous RGB data to external display devices through the LVDS interface.

- Supports FPD link
- Supports single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock, with 7:1 ratio from LVDS data
- to pixel clock, implying up to 560Mbps LVDS data rate. This supports resolutions up to approximately 1366x768p60 or 1280x800p60.
- Supports VESA and JEIDA pixel mapping
- Supports LVDS Transmitter with four 7-bit channels. Each channel sends the 6 pixel bits and one control signal at 7 times the pixel clock rate. The data and control signals are transmitted over an LVDS link.

Note: *MIPI DSI and LVDS interfaces can be swapped to support other SOMs in DSI mode.*
In "DSCM" assembly option DSI and LVDS interface pins are swapped.

8.2.1.1 LVDS0 Signals

Table 5: LVDS Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
180	DSCM	LVDS_CLK_N	0	Differential Pair Negative side Available in SOM with "DSCM" configuration	SOC.A3
182	DSCM	LVDS_CLK_P	0	Differential Pair Positive side Available in SOM with "DSCM" configuration	SOC.B3
184	DSCM	LVDS_D0_N	0	Differential Pair Negative side Available in SOM with "DSCM" configuration	SOC.A5
186	DSCM	LVDS_D0_P	0	Differential Pair Positive side Available in SOM with "DSCM" configuration	SOC.B5
188	DSCM	LVDS_D1_N	0	Differential Pair Negative side Available in SOM with "DSCM" configuration	SOC.A4
190	DSCM	LVDS_D1_P	0	Differential Pair Positive side Available in SOM with "DSCM" configuration	SOC.B4
192	DSCM	LVDS_D2_N	0	Differential Pair Negative side Available in SOM with "DSCM" configuration	SOC.A2
194	DSCM	LVDS_D2_P	0	Differential Pair Positive side Available in SOM with "DSCM" configuration	SOC.B2
183	DSCM	LVDS_D3_N	0	Differential Pair Negative side Available in SOM with "DSCM" configuration	SOC.B1
181	DSCM	LVDS_D3_P	0	Differential Pair Positive side Available in SOM with "DSCM" configuration	SOC.C1
168	No DSCM	LVDS_CLK_N	0	Differential Pair Negative side Available in SOM without "DSCM" configuration	SOC.A3
170	No DSCM	LVDS_CLK_P	0	Differential Pair Positive side Available in SOM without "DSCM" configuration	SOC.B3
161	No DSCM	LVDS_D0_N	0	Differential Pair Negative side Available in SOM without "DSCM" configuration	SOC.A5
163	No DSCM	LVDS_D0_P	0	Differential Pair Positive side Available in SOM without "DSCM" configuration	SOC.B5
160	No DSCM	LVDS_D1_N	0	Differential Pair Negative side Available in SOM without "DSCM" configuration	SOC.A4
162	No DSCM	LVDS_D1_P	0	Differential Pair Positive side Available in SOM without "DSCM" configuration	SOC.B4
164	No DSCM	LVDS_D2_N	0	Differential Pair Negative side Available in SOM without "DSCM" configuration	SOC.A2
166	No DSCM	LVDS_D2_P	0	Differential Pair Positive side Available in SOM without "DSCM" configuration	SOC.B2
165	No DSCM	LVDS_D3_N	0	Differential Pair Negative side Available in SOM without "DSCM" configuration	SOC.B1
167	No DSCM	LVDS_D3_P	0	Differential Pair Positive side Available in SOM without "DSCM" configuration	SOC.C1

8.2.2 DSI

The i.MX 93 SOC support one 4-lane MIPI DSI display with pixels from the LCDIF. The key features of the MIPI DSI (controller and PHY) include:

- Compliant to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
- Maximum resolution limited to resolutions achievable with a 200MHz pixel clock and active pixel rate of 140Mpixel/s with 24-bit RGB. Resolutions up to 1920x1200p60
- Support up to 1.5Gbps data rate per lane in high-speed and 10Mbps in low-speed operation

Note: *MIPI DSI and LVDS interfaces can be swapped to support other SOMs in DSI mode. In "DSCM" assembly option DSI and LVDS interface pins are swapped.*

8.2.2.1 DSI Signals

Table 6: MIPI DSI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
168	DSCM	MIPI_DSI1_CLK_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.D6
170	DSCM	MIPI_DSI1_CLK_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.E6
161	DSCM	MIPI_DSI1_D0_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A6
163	DSCM	MIPI_DSI1_D0_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B6
160	DSCM	MIPI_DSI1_D1_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A7
162	DSCM	MIPI_DSI1_D1_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B7
164	DSCM	MIPI_DSI1_D2_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A8
166	DSCM	MIPI_DSI1_D2_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B8
165	DSCM	MIPI_DSI1_D3_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A9
167	DSCM	MIPI_DSI1_D3_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B9
180	No DSCM	MIPI_DSI1_CLK_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.D6
182	No DSCM	MIPI_DSI1_CLK_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.E6
184	No DSCM	MIPI_DSI1_D0_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A6
186	No DSCM	MIPI_DSI1_D0_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B6
188	No DSCM	MIPI_DSI1_D1_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A7
190	No DSCM	MIPI_DSI1_D1_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B7
192	No DSCM	MIPI_DSI1_D2_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A8
194	No DSCM	MIPI_DSI1_D2_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B8
183	No DSCM	MIPI_DSI1_D3_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.A9
181	No DSCM	MIPI_DSI1_D3_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.B9

8.2.3 LCDIF

The LCD Interface (LCDIF) is a system master that fetches graphics stored in memory and display them on a TFT LCD panel. A wide range of panel sizes is supported and the timing of the interface signals is highly configurable. Graphics are read directly from memory. Graphics may be encoded in a variety of formats to optimize memory usage.

8.2.3.1 LCDIF Signals

Table 7: LCDIF Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
171		lcdif.D[0]	3		SOC.L17
115		lcdif.D[1]	3		SOC.L18
176		lcdif.D[2]	3		SOC.L20
174		lcdif.D[3]	3		SOC.L21
124		lcdif.D[4]	3		SOC.M20
175		lcdif.D[5]	3		SOC.M21
48		lcdif.D[6]	3		SOC.N17
77		lcdif.D[7]	3		SOC.N18
191	No TP	lcdif.D[8]	3		SOC.N20
193	No TP	lcdif.D[9]	3		SOC.N21
187	No TP	lcdif.D[10]	3		SOC.P20
189	No TP	lcdif.D[11]	3		SOC.P21
25		lcdif.D[12]	3		SOC.R21
86		lcdif.D[13]	3		SOC.R20
22		lcdif.D[14]	3		SOC.R18
23		lcdif.D[15]	3		SOC.R17
21		lcdif.D[16]	3		SOC.T20
26		lcdif.D[17]	3		SOC.T21
87		lcdif.D[18]	3		SOC.U18
88		lcdif.D[19]	3		SOC.U20
17		lcdif.D[20]	3		SOC.U21
68		lcdif.D[21]	3		SOC.V21
24		lcdif.D[22]	3		SOC.V20
69		lcdif.D[23]	3		SOC.W21
41		lcdif.DE	3		SOC.J20
43		lcdif.HSYNC	3		SOC.K21
39		lcdif.PCLK	3		SOC.J21
45		lcdif.VSYNC	3		SOC.K20

8.3 Camera Interface

8.3.1 MIPI CSI-2

The i.MX93 SOC supports one 2-lane MIPI CSI2 camera inputs. The key features of the MIPI CSI2 (controller and PHY) include:

- Compliant to MIPI-DSI specification v1.2 and MIPI-DPHY specification v1.2
- Supports up to 2 Rx data lanes (plus 1 Rx clock lane)

8.3.1.1 MIPI-CSI2 Signals

Table 8: MIPI-CSI2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
137		MIPI_CSI1_CLK_N	137	Differential Pair Negative side	SOC.D10
135		MIPI_CSI1_CLK_P	135	Differential Pair Positive side	SOC.E10
121		MIPI_CSI1_D0_N	121	Differential Pair Negative side	SOC.A11
119		MIPI_CSI1_D0_P	119	Differential Pair Positive side	SOC.B11
123		MIPI_CSI1_D1_N	123	Differential Pair Negative side	SOC.A10
125		MIPI_CSI1_D1_P	125	Differential Pair Positive side	SOC.B10

8.3.2 ISI - Image Sensing Interface

The ISI module interfaces to a pixel link source to obtain the image data for processing in its pipeline channel. The pipeline processes the image line from a configured source and performs one or more functions that are configured by software, such as down scaling, color space conversion, de-interlacing, alpha insertion, and cropping and rotation (horizontal and vertical). The processed image is stored into programmable memory locations.
The ISI module implements limited flow control mechanism to control output from its internal buffer flushing or sourcing an image ROM memory. Depending on the format type, the ISI is capable of processing and storing one line of pixels from the incoming

The key features of the ISI include:

- Up to 2K resolution at 30 or 60 fps (24bpp) on each channel.
- Input sources:
  - 1 pixel link interface that can interface to 1 camera sensor.
  - System memory (AXI master, internally converted to pixel link interface).
- Each processing pipeline or channel can be assigned to the same or different pixel input source.
- Stream multiplexing
  - Simple de-interlacing methods supported for interlaced input sources:
    - Weaving
- Stream manipulation
  - Supported pixel formats of images to be stored into memory
    - RAW8, RAW10, RAW12, RAW14, RAW16, RAW32
    - RGB888, BGR888, RGB565, RGB 10-bit, BGR 10-bit
    - YUV444, YUV422, YUV420 (8-bit, 10-bit, 12-bit) in planar or semi-planar formats

        - Plus more formats listed in the description of FORMAT field in the channel's IMG_CTRL register
    - Downscaling of input image via decimation and bilinear filtering
        - Decimation by 2, 4, or 8 supported
        - Bilinear filter further downscales by 1.0 to 2.0 (fractional downscaling)
    - Color Space Conversion (CSC)
        - RGB, YUV, YCbCr
        - User defined color space matrix based conversion
    - Alpha channel insertion for RGB formats
        - Global alpha value
    - Separate rectangular region of interest (ROI) alpha value. ROI alpha value has higher priority than global alpha value.
        - Up to 4 ROI non-overlapping rectangles supported
    - Mirroring (Image fip): Horizontal and vertical flipping supported.
    - Frame awareness and frame skipping
        - Clean frame start and shutdown based on HSYNC and VSYNC
        - Buffer overrun protection
        - Buffer underrun deterministic behavior
- Stream output options
    - Output to memory
        - Input source is converted to and processed by the processing pipeline as YUV444 or RGB.
        - Processed images are outputted from pipeline and stored into memory location specified by software.
        - Full line storage is available at processing channel output before outputting data to AXI. This storage can automatically split or combine depending on the output format being used.
        - Dual buffered addresses are used in ping pong fashion with active buffer status indication.
        - Line and frame stored interrupt status are used for software to track progress of frame.
- Flow control
    - Panic indication is used for software and device to increase priority of its write transactions to avoid potential overflow in output buffers. Software can configure thresholds for panic indication.
    - When pixels are sourced from memory or input line buffers are flushed, software can select to program the rate at which pixels are sent out. By default, one pixel is sent out per clock.
    - Back pressure mechanism is used to stall the channel pipeline during line buffer flushing and sourcing image from memory when AXI bus is unable accept data and the output buffers are low on storage.
- Metadata processing
    - The embedded data from the sensor can be processed and written out.

8.3.2.1 ISI Signals

Table 9: ISI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		isi.D[0]	2		SOC.J20
174		isi.D[1]	2		SOC.L21
124		isi.D[2]	2		SOC.M20
175		isi.D[3]	2		SOC.M21
48		isi.D[4]	2		SOC.N17
77		isi.D[5]	2		SOC.N18
187	No TP	isi.D[6]	2		SOC.P20
189	No TP	isi.D[7]	2		SOC.P21
86		isi.D[8]	2		SOC.R20
22		isi.D[9]	2		SOC.R18
45		isi.FRAME_VALID	2		SOC.K20
43		isi.LINE_VALID	2		SOC.K21
39		isi.PCLK	2		SOC.J21

8.4 Ethernet Interface

The i.MX 93 SOC implements Two Ethernet controllers both capable of simultaneous operation. One 1G-bit Ethernet with AVB support (ENET) plus a separate 1Gbit Ethernet QoS with TSN support.

ENET_QOS (Ethernet Quality of Service) - Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588

ENET1 - Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

8.4.1 ENET_QOS (Ethernet Quality of Service)

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The VAR-SOM-MX93 includes an on SOM a Gigabit PHY (Analog Devices ADIN1300) connected to ENET_QOS RGMII interface signals. External connector and magnetics should be implemented on carrier board to complete the interface to the media.
- **"no EC" configuration** – The VAR-SOM-MX93 exposes the ENET_QOS RGMII/RMII interface signals to the SO-DIMM connector and ENET_QOS pins are referenced to 1.8V.

8.4.1.1 Ethernet PHY

The on SOM AR8033 / Analog Devices ADIN1300 Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.
PHY LINK LEDs 10/100 and 1000 combined on SOM to one signal 10/100/1000.

The Following External Gigabit magnetics are required to complete the Ethernet PHY interface to the media.

Table 10: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 11: Ethernet PHY Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
15	EC	ETH0_LED_ACT		Signal source is Ethernet PHY Ethernet PHY Activity LED, active low Includes on SOM 10K pull up	ADIN1300BCPZ.21
16	EC	ETH0_LED_LINK		Signal source is Ethernet PHY Ethernet PHY Link LED, active low Includes on SOM open drain inverter	ADIN1300BCPZ.26
5	EC	ETH0_MDI_A_M		Signal source is Ethernet PHY	ADIN1300BCPZ.13
3	EC	ETH0_MDI_A_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300BCPZ.12
11	EC	ETH0_MDI_B_M		Signal source is Ethernet PHY	ADIN1300BCPZ.15
9	EC	ETH0_MDI_B_P		Differential Pair Positive side	ADIN1300BCPZ.14
6	EC	ETH0_MDI_C_M		Signal source is Ethernet PHY	ADIN1300BCPZ.17
4	EC	ETH0_MDI_C_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300BCPZ.16
12	EC	ETH0_MDI_D_M		Signal source is Ethernet PHY	ADIN1300BCPZ.19
10	EC	ETH0_MDI_D_P		Differential Pair Positive side Signal source is Ethernet PHY	ADIN1300BCPZ.18
141		ETH_INT_1V8		1.8V level signal	ADIN1300BCPZ.22

Table 12: ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.4.1.2 ENET_QOS Signals

Table 13: ENET_QOS RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
4	No EC	enet_qos.RGMII_RD0	0	1.8V level signal	AA8
6	No EC	enet_qos.RGMII_RD1	0	1.8V level signal	Y9
10	No EC	enet_qos.RGMII_RD2	0	1.8V level signal	AA9
12	No EC	enet_qos.RGMII_RD3	0	1.8V level signal	Y10
15	No EC	enet_qos.RGMII_RX_CTL	0	1.8V level signal	Y8
16	No EC	enet_qos.RGMII_RXC	0	1.8V level signal	AA7
11	No EC	enet_qos.RGMII_TD0	0	1.8V level signal	W11
9	No EC	enet_qos.RGMII_TD1	0	1.8V level signal	T12
5	No EC	enet_qos.RGMII_TD2	0	1.8V level signal	U12
3	No EC	enet_qos.RGMII_TD3	0	1.8V level signal	V12
1	No EC	enet_qos.RGMII_TX_CTL	0	1.8V level signal	V10
58	No EC	enet_qos.RGMII_TXC	0	1.8V level signal	U10
16	No EC	enet_qos.RX_ER	1	1.8V level signal	AA7
58	No EC	enet_qos.TX_ER	1	1.8V level signal	U10
5	No EC	INPUT=enet_qos.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_CLK_ROOT	1	1.8V level signal	U12
80		enet_qos.1588_EVENT0_IN	1	Can be 3.3V or 1.8V depending on SD Card type 3.3V by default. Referenced to LDO5 voltage.	Y17
60		enet_qos.1588_EVENT0_OUT	1	Can be 3.3V or 1.8V depending on SD Card type 3.3V by default. Referenced to LDO5 voltage.	AA19
74		enet_qos.MDC	0	3.3V voltage levels. Includes on SOM 1.8V to 3.3V bidirectional voltage translator.	AA11
30		enet_qos.MDIO	0	3.3V voltage levels. Includes on SOM 1.8V to 3.3V bidirectional voltage translator.	AA10

8.4.2 ENET2

ENET2 RGMII/RMII interface signals are always exported through SO-DIMM connector. Signals, in conjunction to MDIO signals exported from SO-DIMM connector, they can be used to interface an external Ethernet PHY.

ENET2 pins are referenced to 1.8V.

8.4.2.1 ENET2 Signals

Table 14: ENET2 RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
122		enet2.RGMII_RD0	0	1.8V level signal	SOC.AJ9
81		enet2.RGMII_RD1	0	1.8V level signal	SOC.AH8
71		enet2.RGMII_RD2	0	1.8V level signal	SOC.AC10
54		enet2.RGMII_RD3	0	1.8V level signal	SOC.AF10
120		enet2.RGMII_RX_CTL	0	1.8V level signal	SOC.AE12
57		enet2.RGMII_RXC	0	1.8V level signal	SOC.AH9
73		enet2.RGMII_TD0	0	1.8V level signal	SOC.AJ8
177		enet2.RGMII_TD1	0	1.8V level signal	SOC.AD10
56		enet2.RGMII_TD2	0	1.8V level signal	SOC.AE10
55		enet2.RGMII_TD3	0	1.8V level signal	SOC.AH10
113		enet2.RGMII_TX_CTL	0	1.8V level signal	SOC.AH12
96		enet2.RGMII_TXC	0	1.8V level signal	SOC.AF12
64		enet2.1588_EVENT0_IN	1	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AJ12
62		enet2.1588_EVENT0_OUT	1	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AJ11
63		enet2.1588_EVENT1_IN	1	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AJ10
61		enet2.1588_EVENT1_OUT	1	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AH11

8.5 Wi-Fi & BT

The VAR-SOM-MX93 contains a certified high-performance Wi-Fi (Single or Dual Band option) and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR
- BLE 5.2 capabilities
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SOM-MX93 internal Wi-Fi and BT connectivity.

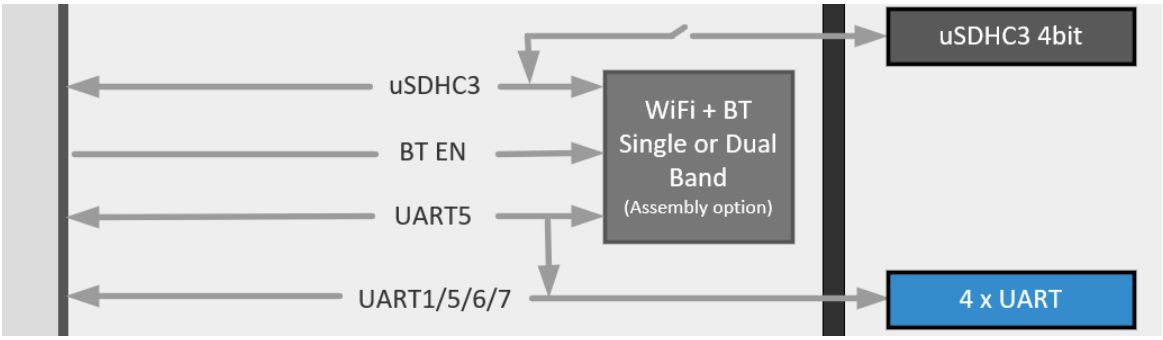


Figure 3: VAR-SOM-MX93 Wi-Fi & BT Internal Connection

8.5.1 Interface Implementation Options

8.5.1.1 Module Configuration with "WBD" or "WB" Option

- System use: Wi-Fi and Bluetooth.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT module (using GPIO4.IO[15]).
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT module (using GPIO4.IO[15]).

8.5.1.2 Module Configuration without "WBD" or "WB" Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.

8.5.2 Bluetooth Interface Signals

Table 15: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		uart5.RTS_B	6	Used internally with "WBD" or “WB” Function can be released if BT Function disabled Always exposed	SOC.W2
51		uart5.CTS_B	6	Used internally with "WBD" or “WB” Function can be released if BT Function disabled Always exposed	SOC.Y1
52		uart5.TX	6	Used internally with "WBD" or “WB” Function can be released if BT Function disabled Always exposed	SOC.Y2
53		uart5.RX	6	Used internally with "WBD" or “WB” Function can be released if BT Function disabled Always exposed	SOC.W1

8.5.3 Wakeup signals

The VAR-SOM-MX93 exposes Wi-Fi and BT wakeup signals of the modules on the SOM. The voltage levels of the signals are 1.8V.
The purpose of these signals is to be connected externally to some GPIO lines and use as a wakeup source for the main CPU.
For implementation please check out the Wi-Fi module datasheet.

Table 16: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
128	WB or WBD	WIFI_HOST_WAKE		1.8V level signal	450-01159R.131, 450-0162R.17
130	WB or WBD	BT_DEV_WAKE		1.8V level signal	450-01159R.56, 450-0162R.47
134	WB or WBD	BT_HOST_WAKE		1.8V level signal	450-01159R.57, 450-0162R.46

8.6 Ultra-Secured Digital Host Controller

The VAR-SOM-MX93 exposes the uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.
Key features of uSDHC2:

- SD/SDIO standard, up to version 3.0.
- compliance with 200 MHz SDR signaling to support up to 100 MB/sec
- 1.8 V and 3.3 V operation
- Support for SDXC (extended capacity)

8.6.1 uSDHC1 Signals

uSDHC controller, uSDHC1, is used internally for the eMMC storage chip on the SOM.

8.6.2 uSDHC2 Signals

uSDHC2 pins are referenced to LDO5 power supply of the PMIC.
By default, this LDO supplies 3.3V in order to allow proper boot from SD Card.
The system uses SD2_VSELECT pin in order to switch between 3.3V and 1.8V.
This pin functionality can be changed to gpio3.IO[19] and controlled programmatically.

- Low state will select 3.3V interface
- High state will select 1.8V interface

Table 17: uSDHC2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
80		usdhc2.CD_B	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.Y17
60		usdhc2.CLK	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AA19
64		usdhc2.CMD	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.Y19
62		usdhc2.DATA0	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.Y18
63		usdhc2.DATA1	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AA18
61		usdhc2.DATA2	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.Y20
65		usdhc2.DATA3	0	3.3V by default. Referenced to LDO5 voltage. Can be 3.3V or 1.8V depending on SD Card type.	SOC.AA20

8.6.3 uSDHC3 Signals

uSDHC controller, uSDHC3, is used internally for the Wi-Fi interface on the SOM.
It can be used when the Wi-Fi is not assembled via two different pin locations.
One location operates in 3.3V voltage levels and other operates in 1.8V voltage levels.
3.3V level group is always exposed, but uSDHS3 function cannot be used in parallel with Wi-Fi.
1.8V level group exposed only on SOMs without Wi-Fi module assembled.

Table 18: uSDHC3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
87		usdhc3.CLK	1		SOC.U18
88		usdhc3.CMD	1		SOC.U20
17		usdhc3.DATA0	1		SOC.U21
68		usdhc3.DATA1	1		SOC.V21
24		usdhc3.DATA2	1		SOC.V20
69		usdhc3.DATA3	1		SOC.W21
145	No WB or WBD	usdhc3.CLK	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.V16
147	No WB or WBD	usdhc3.CMD	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.U16
84	No WB or WBD	usdhc3.DATA0	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.T16
31	No WB or WBD	usdhc3.DATA1	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.V14
33	No WB or WBD	usdhc3.DATA2	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.U14
35	No WB or WBD	usdhc3.DATA3	0	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.T14

8.7 USB 2.0

The VAR-SOM-MX93 consists Two USB controllers and PHYs that support USB 2.0.

8.7.1 USB Port1 Interface Signals

Table 19: USB 3.0/2.0 Port 1 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
114		usb1.D_N	0	Differential Pair Negative side USB OTG capable	SOC.A14
116		usb1.D_P	0	Differential Pair Positive side USB OTG capable	SOC.B14
94		usb1.ID	0	USB PHY ID pin, No GPIO function USB OTG ID alternative signal location. "Low" means the SoC is Host role "High" means the SoC is Peripheral role. Pin referenced to 1.8V.	SOC.C11
106		usb1.VBUS	0	USB PHY power pin; 5V tolerant	F12
9	No EC	usb1.OTG_OC	3	1.8V level signal	SOC.T12
30	No EC	usb1.OTG_PWR	3	3.3V voltage levels. Goes through bidirectional level translator	SOC.AA10
74	No EC	usb1.OTG_ID	3	3.3V voltage levels. Goes through bidirectional level translator	SOC.AA11

Note: *Usage of native USB_ID in i.MX93 requires patches not included in NXP formal release. Pin referenced to 1.8V. For simple OTG implementation, use a CC Logic chip and connect to GPIO (see Symphony-Board implementation). USB1_ID can be left floating if not used.*

8.7.2 USB Port2 Interface Signals

Table 20: USB 2.0 Port 2 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
108		USB2_D_N	0	Differential Pair Negative side	SOC.A15
110		USB2_D_P	0	Differential Pair Positive side	SOC.B15
104		USB2_VBUS	0	USB PHY power pin; 5V tolerant	SOC.E14
3	No EC	usb2.OTG_ID	3	1.8V level signal	SOC.V12
5	No EC	usb2.OTG_OC	3	1.8V level signal	SOC.U12
15	No EC	usb2.OTG_PWR	3	1.8V level signal	SOC.Y8

8.8 Audio

The VAR-SOM-MX93 features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces:
  - SAI-1 supports to up to 16-channels TX (8 lanes) and 16-channels RX (8 lanes) at 768KHz/32-bit
  - SAI-2/5 supports to up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 768KHz/32-bit
  - SAI-3 supports up to 4-channels TX (2 lanes) and 4-channels RX (2 lanes) at 768KHz/32-bit
  - SAI-6 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 768KHz/32-bit when multiplexed on SAI1, or up to 384kHz/32-bit when multiplexed on Ethernet primary pins
  - SAI-7 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384KHz/32-bit
- PDM supporting up to 8-channels (4 lanes)
- S/PDIF Input and Output, including a new Raw Capture input mode
- Hifi4 Audio DSP, operating up to 800 MHz

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via SAI3 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

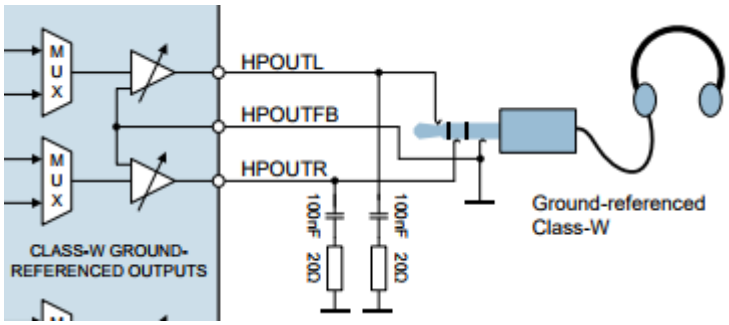


Figure 4: WM8904 Headphone connectivity

8.8.1 WM8904CGEFL Audio Codec

8.8.1.1 Audio Codec Signals

Table 21: Analog audio Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
195		AGND		Audio Ground	AGND
18	AC	DMIC_CLK		Signal source is Audio Codec Digital microphone clock output	WM8904.1
20	AC	DMIC_DATA		Signal source is Audio Codec Digital microphone data input; Divided internally by 475 Ohm resistors to match Codec input levels	WM8904.27
198	AC	HPLOUT		Signal source is Audio Codec Left headphone output (line or headphone output) Includes on SOM audio filter	WM8904.13
196	AC	HPOUTFB		Signal source is Audio Codec Headphone output ground loop noise rejection feedback	WM8904.14
200	AC	HPROUT		Signal source is Audio Codec Right headphone output (line or headphone output) Includes on SOM audio filter	WM8904.15
197	AC	LINEIN1_LP		Signal source is Audio Codec Left channel input	WM8904.26
199	AC	LINEIN1_RP		Signal source is Audio Codec Right channel input	WM8904.24

8.8.2 Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

8.8.2.1 SAI Signals

Table 22: Serial Audio Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
20	No AC	sai1.MCLK	4		SOC.F20
197	No AC	sai1.RX_BCLK	4		SOC.D21
198	No AC	sai1.RX_DATA[0]	0		SOC.H20
196	No AC	sai1.RX_SYNC	4		SOC.D20
200	No AC	sai1.TX_BCLK	0		SOC.G20
18	No AC	sai1.TX_DATA[0]	0		SOC.H21
199	No AC	sai1.TX_SYNC	0		SOC.G21
71		sai2.MCLK	2	1.8V level signal	SOC.AA5
55		sai2.RX_DATA[0]	2	1.8V level signal	SOC.T10
56		sai2.RX_DATA[1]	2	1.8V level signal	SOC.V8
177		sai2.RX_DATA[2]	2	1.8V level signal	SOC.U8
73		sai2.RX_DATA[3]	2	1.8V level signal	SOC.T8
96		sai2.TX_BCLK	2	1.8V level signal	SOC.U6
120		sai2.TX_DATA[0]	2	1.8V level signal	SOC.Y4
57		sai2.TX_DATA[1]	2	1.8V level signal	SOC.AA3
122		sai2.TX_DATA[2]	2	1.8V level signal	SOC.AA4
81		sai2.TX_DATA[3]	2	1.8V level signal	SOC.Y5
113		sai2.TX_SYNC	2	1.8V level signal	SOC.V6
86		sai3.MCLK	1		SOC.R20
22		sai3.RX_BCLK	1		SOC.R18
26		sai3.RX_BCLK	7		SOC.T21
21		sai3.RX_DATA[0]	1		SOC.T20
23		sai3.RX_SYNC	1		SOC.R17
191		sai3.RX_SYNC	7		SOC.N20
25		sai3.TX_BCLK	1		SOC.R21
26		sai3.TX_DATA[0]	1		SOC.T21
23		sai3.TX_DATA[0]	7		SOC.R17
24		sai3.TX_SYNC	7		SOC.V20

8.8.3 PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX93 SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

The PDM Microphone Interface module is composed of:

- A decimation filter by channel that:
  - Consists, internally, of a cascade integrator comb (CIC) filter, a DC remover, and half-band filters. The filtering results are stored in individual FIFOs (a FIFO per channel). These FIFOs have overflow and underflow detectors to deliver an error interrupt request.
  - Implements a low-pass filter in the audio band (20 Hz–20.0 kHz @48 kHz output sampling rate by default) with a configurable decimation rate. You can implement it using a series of CIC, half-band, and DC remover filters.
  - Stores its output into a FIFO buffer, and each FIFO is mapped to MICFIL Output Result (DATACH0 - DATACH7). It is possible to generate either an interrupt or a DMA request when, in each FIFO of all enabled channels, the number of data stored surpasses a configured watermark.
  - Also, independently on decimation filters, there is a Hardware Voice Activity Detector (HWVAD) which implements voice-detection algorithms to generate wake-up interrupts.
- A shared time generator unit that:
  - Delivers the PDM_CLK to all microphones that must operate at the same clock frequency. Each input interface receives a time multiplexed PDM bitstream from two PDM microphones and it separates audio information in two channels: left (0) and right (1). Every decimation filter, corresponding to its channel, does this processing.
  - Generates the PDM_CLK to the microphones. This clock is the same and is active for all the PDM microphones, which means, it is not possible to turn off the PDM_CLK only for one single microphone.
- An input interface for each pair of PDM microphones
- A FIFO by channel
- A shared DMA interface, interrupt interface, and bus interface
- A shared interface to the chip
- A Hardware Voice Activity Detector (HWVAD)

PDM block main features are:

- Decimation filters:
  - Fixed-point filtering
  - 24-bit PCM audio output
  - Internal clock divider for a programmable PDM clock generation
- Full or partial set of channel operations with individual enable controls
- Programmable decimation rate
- Programmable DC remover
- Programmable DC remover at output
- Range adjustment capability

- FIFOs with interrupt and DMA capability: each FIFO having a length of 32 entries
- HWVAD, equipped with:
    - Interrupt capability
    - Zero-Crossing Detection (ZCD) option

Table 23: PDM Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
21		pdm.BIT_STREAM[0]	2		SOC.T20
46		pdm.BIT_STREAM[0]	0		SOC.J17
115		pdm.BIT_STREAM[0]	2		SOC.L18
72		pdm.BIT_STREAM[1]	0		SOC.G18
24		pdm.BIT_STREAM[1]	2		SOC.V20
176		pdm.BIT_STREAM[1]	2		SOC.L20
191	TP	pdm.BIT_STREAM[2]	2		SOC.N20
25		pdm.BIT_STREAM[2]	2		SOC.R21
193	TP	pdm.BIT_STREAM[3]	2		SOC.N21
23		pdm.BIT_STREAM[3]	2		SOC.R17
26		pdm.CLK	2		SOC.T21
44		pdm.CLK	0		SOC.G17
171		pdm.CLK	2		SOC.L17

8.8.4 MQS - Medium Quality Sound

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip.

Table 24: MQS Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
44		mqs1.LEFT	1		SOC.G17
199	No AC	mqs1.LEFT	4		SOC.G21
46		mqs1.RIGHT	1		SOC.J17
198	No AC	mqs1.RIGHT	4		SOC.H20
53		mqs2.LEFT	1	1.8V level signal. UART can be used if BT disabled	SOC.W1
54		mqs2.LEFT	3	1.8V level signal	SOC.Y6
65		mqs2.LEFT	2	3.3V by default. Referenced to LDO5 voltage.	SOC.AA20
52		mqs2.RIGHT	1	1.8V level signal. UART can be used if BT disabled	SOC.Y2
61		mqs2.RIGHT	2	3.3V by default. Referenced to LDO5 voltage.	SOC.Y20
71		mqs2.RIGHT	3	1.8V level signal	SOC.AA5

8.8.5 SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

Table 25: SPDIF Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
81		spdif1.IN	1		SOC.Y5
54		spdif1.OUT	1		SOC.Y6
87		spdif1.IN	2		SOC.U18
88		spdif1.OUT	2		SOC.U20
54		spdif1.IN	2		SOC.Y6

8.9 Resistive Touch

The VAR-SOM-MX93 features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option
when not assembled, ECSPI8 SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

8.9.1.1 Resistive Touch Signals

Table 26: Serial Resistive Touch Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	TP	TS_X-		Signal source is Resistive Touch controller	TSC2046.8
189	TP	TS_X+		Signal source is Resistive Touch controller	TSC2046.6
191	TP	TS_Y+		Signal source is Resistive Touch controller	TSC2046.7
193	TP	TS_Y-		Signal source is Resistive Touch controller	TSC2046.9

8.10 LPUART

The VAR-SOM-MX93 exposes up to seven LPUART interfaces some of which are multiplexed with other peripherals. UART5 is used on SOM for Bluetooth interface and can be accessible only if the BT is disabled or on SOM without ***"WBD" and "WB" Configuration***.

The LPUART includes the following features:

- Full-duplex, standard NRZ format
- Programmable baud rates (13-bit modulo divider) with a configurable oversampling ratio (OSR)
- Asynchronous operations of transmit and receive baud rates with respect to the bus clock:
    - Baud rate can be configured independently of the bus clock frequency.
    - Operation in Low-Power modes is supported.
- Interrupt, DMA, or polled operations:
    - Transmit data empty and transmission complete
    - Receive data full
    - Receive overrun, parity error, framing error, and noise error
    - Idle receiver detect
    - Active edge on receive pin
    - Break detect supporting LIN
    - Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit, or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Support for three receiver wakeup methods:
    - Idle line wakeup
    - Address mark wakeup
    - Receive data match
- Automatic address matching to reduce ISR overhead:
    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit and 11-bit break character generation
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64, or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with a programmable pulse width
- Independent FIFO structure for transmit and receive functions:
    - Separate configurable watermarks for receive and transmit requests
    - Option for receiver to assert request after a configurable number of idle characters, if receive FIFO is not empty

Unlike other i.MX8M based SOMs the direction of the UART lines cannot be programmed. The following table shows the direction of signals of i.MX93 LPUARTs

Table 27: LPUART I/O Direction

Signal	Direction
uartX.TX	Output
uartX.RX	Input
uartX.RTS_B	Output
uartX.CTS_B	Input

8.10.1 LPUART1 Signals

Table 28: LPUART1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
20	No AC	uart1.CTS_B	1		SOC.F20
92		uart1.DCB_B	2		SOC.C20
200	No AC	uart1.DSR_B	3		SOC.G20
18	No AC	uart1.DTR_B	3		SOC.H21
90		uart1.RIN_B	2		SOC.C21
83		uart1.RX	0		SOC.E20
85		uart1.TX	0		SOC.E21

8.10.2 LPUART3 Signals

Table 29: LPUART3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
25		uart3.CTS_B	4		SOC.R21
86		uart3.RTS_B	4		SOC.R20
189	No TP	uart3.RX	1		SOC.P21
187	No TP	uart3.TX	1		SOC.P20

8.10.3 LPUART4 Signals

Table 30: LPUART4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
25		uart4.CTS_B	6		SOC.R21
71		uart4.CTS_B	1	1.8V level signal	SOC.AA5
120		uart4.DSR_B	1	1.8V level signal	SOC.Y4
113		uart4.DTR_B	1	1.8V level signal	SOC.V6
86		uart4.RTS_B	6		SOC.R20

Pin#	Assy	Pin Function	Alt#	Notes	Ball
177		uart4.RTS_B	1	1.8V level signal	SOC.U8
122		uart4.RX	1	1.8V level signal	SOC.AA4
189	No TP	uart4.RX	6		SOC.P21
73		uart4.TX	1	1.8V level signal	SOC.T8
187	No TP	uart4.TX	6		SOC.P20

8.10.4 LPUART5 Signals

Table 31: LPUART5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
45		uart5.CTS_B	5		SOC.K20
51		uart5.CTS_B	6	1.8V level signal. UART can be used if BT disabled	SOC.Y1
43		uart5.RTS_B	5		SOC.K21
50		uart5.RTS_B	6	1.8V level signal. UART can be used if BT disabled. Has an internal 10K pull down	SOC.W2
41		uart5.RX	5	Cannot be configured as I2C3	SOC.J20
53		uart5.RX	6	1.8V level signal. UART can be used if BT disabled	SOC.W1
39		uart5.TX	5	Cannot be configured as I2C3	SOC.J21
52		uart5.TX	6	1.8V level signal. UART can be used if BT disabled	SOC.Y2

8.10.5 LPUART6 Signals

Table 32: LPUART6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
176		uart6.CTS_B	5		SOC.L20
174		uart6.RTS_B	5		SOC.L21
115		uart6.RX	5		SOC.L18
171		uart6.TX	5		SOC.L17

8.10.6 LPUART7 Signals

Table 33: LPUART7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
48		uart7.CTS_B	5		SOC.N17
77		uart7.RTS_B	5		SOC.N18
175		uart7.RX	5		SOC.M21
124		uart7.TX	5		SOC.M20

8.10.7 LPUART8 Signals

Table 34: LPUART8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	No TP	uart8.CTS_B	5		SOC.P20
189	No TP	uart8.RTS_B	5		SOC.P21
193	No TP	uart8.RX	5		SOC.N21
191	No TP	uart8.TX	5		SOC.N20

8.11 Flexible Controller Area Network

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1:2015 standard and CAN 2.0 B protocol specifications

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

8.11.1 FLEXCAN1 Signals

Table 35: FLEXCAN1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
46		can1.RX	6		SOC.J17
200	No AC	can1.RX	4		SOC.G20
18	No AC	can1.TX	4		SOC.H21
44		can1.TX	6		SOC.G17

8.11.2 FLEXCAN2 Signals

Table 36: FLEXCAN2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
5	No EC	can2.RX	2	1.8V level signal	SOC.U12
52		can2.RX	3	1.8V level signal.	SOC.Y2
63		can2.RX	2	3.3V by default. Referenced to LDO5 voltage.	SOC.AA18
69		can2.RX	2		SOC.W21
3	No EC	can2.TX	2	1.8V level signal	SOC.V12
53		can2.TX	3	1.8V level signal.	SOC.W1
62		can2.TX	2	3.3V by default. Referenced to LDO5 voltage.	SOC.Y18
68		can2.TX	2		SOC.V21

8.12 LPSPI - Low Power Serial Peripheral Interface

The VAR-SOM-MX93 exposes up to 7 LPSPI interfaces.

LPSPI provides an efficient interface to a SPI bus, either as a master or slave. A SPI bus is a synchronous serial communication interface used in embedded systems. It is typically used to perform short distance communications between microcontrollers and peripheral devices, on printed circuit boards. Typical applications include interfacing to Secure Digital cards and LCD displays.

Key features of the ECSPI include:

- Requires minimal CPU overhead, with DMA offloading of FIFO register accesses
- Continues operating in Stop mode, if configured to do so and an appropriate clock is available
- Supports DMA accesses and generates DMA requests
- 32-bit word size
- Configurable clock polarity and phase
- Master mode—supports up to 2 peripheral chip selects
- Slave mode
- 8-word transmit and command FIFO
- 8-word receive FIFO
- Flexible timing parameters in Master mode, including SCK frequency and duty cycle, and delays between PCS and SCK edges
- Continuous transfer option to keep PCS asserted across multiple frames
- Full-duplex transfers support 1-bit transmit and receive on each clock edge
- Half-duplex transfers support:
    - 1-bit transmit or receive on each clock edge
- Receive data match logic supports discard of non-matching data and interrupt on data match

Note: *For interacting multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select. Examples can be found in our DTS files.*

8.12.1 LPSPI1 Signals

Table 37: LPSPI1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
199	No AC	spi1.PCS0	2		SOC.G21
46		spi1.PCS1	2		SOC.J17
18	No AC	spi1.SCK	2		SOC.H21
200	No AC	spi1.SIN	2		SOC.G20
198	No AC	spi1.SOUT	2		SOC.H20

8.12.2 LPSPI3 Signals

Table 38: LPSPI3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
124		spi3.PCS0	1		SOC.M20
174		spi3.PCS1	1		SOC.L21
77		spi3.SCK	1		SOC.N18
175		spi3.SIN	1		SOC.M21
48		spi3.SOUT	1		SOC.N17

8.12.3 LPSPI4 Signals

Table 39: LPSPI4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
22		spi4.PCS0	5		SOC.R18
86		spi4.PCS1	5		SOC.R20
25		spi4.PCS2	5		SOC.R21
26		spi4.SCK	5		SOC.T21
23		spi4.SIN	5		SOC.R17
21		spi4.SOUT	5		SOC.T20

8.12.4 LPSPI5 Signals

Table 40: LPSPI5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
22		spi5.PCS0	4		SOC.R18
69		spi5.PCS1	6		SOC.W21
26		spi5.SCK	4		SOC.T21
23		spi5.SIN	4		SOC.R17
21		spi5.SOUT	4		SOC.T20

8.12.5 LPSPI6 Signals

Table 41: LPSPI6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
39		spi6.PCS0	4		SOC.J21
17		spi6.PCS1	6		SOC.U21
43		spi6.SCK	4		SOC.K21
41		spi6.SIN	4		SOC.J20
45		spi6.SOUT	4		SOC.K20

8.12.7 LPSPI7 Signals

Table 42: LPSPI7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
171		spi7.PCS0	4		SOC.L17
68		spi7.PCS1	6		SOC.V21
174		spi7.SCK	4		SOC.L21
115		spi7.SIN	4		SOC.L18
176		spi7.SOUT	4		SOC.L20

8.12.8 LPSPI8 Signals

Table 43: LPSPI8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
191	No TP	spi8.PCS0	4		SOC.N20
24		spi8.PCS1	6		SOC.V20
189	No TP	spi8.SCK	4		SOC.P21
193	No TP	spi8.SIN	4		SOC.N21
187	No TP	spi8.SOUT	4		SOC.P20

8.13 FlexSPI - Flexible Serial Peripheral Interface

The VAR-SOM-MX93 exposes one FlexSPI module which can be used to interface external serial flash devices.

The module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- DMA support
- Memory mapped read access to connected flash devices

Note: *FlexSPI signals are available on SOM without Wi-Fi module assembled.*
FlexSPI signals are referenced to 1.8v.

8.13.1 FlexSPI Signals

Table 44: FlexSPI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
84	No WB or WBD	flexspi.A_DATA[0]	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.T16
31	No WB or WBD	flexspi.A_DATA[1]	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.V14
33	No WB or WBD	flexspi.A_DATA[2]	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.U14
35	No WB or WBD	flexspi.A_DATA[3]	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.T14
145	No WB or WBD	flexspi.A_SCLK	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.V16
147	No WB or WBD	flexspi.A_SS0_B	1	1.8V level signal USDHC3 cannot be used on WBD or WB	SOC.U16

8.14 TPM - Timer/PWM Module

The VAR-SOM-MX93 exports up to 6 TPM channels.
The TPM (Timer/PWM Module) is a 4-channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The counter, compare and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

PWM Features:

- TPM clock mode is selectable
  - Can increment on every edge of the asynchronous counter clock
  - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 32-bit TPM counter
  - It can be a free-running counter or modulo counter
  - The counting can be up or up-down
- Includes 4 channels that can be configured as follows:
  - Input capture mode: the capture can occur on rising edges, falling edges or both edges
  - Output compare mode: the output signal can be set, cleared, pulsed, or toggled on match
- Edge-aligned or center-aligned PWM mode for all channels
- Support the generation of an interrupt and/or DMA request per channel
- Support the generation of an interrupt and/or DMA request when the counter overflows
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
  - The counter can also optionally stop incrementing on counter overflow
- Support the generation of hardware triggers when the counter overflows and per channel

8.14.1 TPM Signals

Table 45: TPM Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
83		tpm1.CH0	3		SOC.E20
85		tpm1.CH1	3		SOC.E21
20	No AC	tpm1.CH2	3		SOC.F20
46		tpm1.EXTCLK	3		SOC.J17
92		tpm2.CH0	3		SOC.C20
90		tpm2.CH1	3		SOC.C21
196	No AC	tpm2.CH2	3		SOC.D20
197	No AC	tpm2.CH3	3		SOC.D21
72		tpm2.EXTCLK	3		SOC.G18
171		tpm3.CH0	1		SOC.L17
21		tpm3.CH1	6		SOC.T20
191	No TP	tpm3.CH2	1		SOC.N20
17		tpm3.CH3	4		SOC.U21
175		tpm3.EXTCLK	4		SOC.M21
115		tpm4.CH0	1		SOC.L18
26		tpm4.CH1	6		SOC.T21
193	No TP	tpm4.CH2	1		SOC.N21
68		tpm4.CH3	4		SOC.V21
48		tpm4.EXTCLK	4		SOC.N17
176		tpm5.CH0	1		SOC.L20
87		tpm5.CH1	4		SOC.U18
22		tpm5.CH2	6		SOC.R18
24		tpm5.CH3	4		SOC.V20
77		tpm5.EXTCLK	4		SOC.N18
124		tpm6.CH0	4		SOC.M20
88		tpm6.CH1	4		SOC.U20
23		tpm6.CH2	6		SOC.R17
69		tpm6.CH3	4		SOC.W21
87		tpm6.EXTCLK	5		SOC.U18

8.15 LPI2C - Low Power Inter-Integrated Circuit

The VAR-SOM-MX93 exposes up to seven I2C Interfaces provides access to external serial devices.

The I2C (Inter-Integrated Circuit) serial bus is multi-controller, multi-target, packet-switched, and single-ended, and is often used to attach microcontroller ICs to lower-speed peripheral ICs.

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target. The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 3. The SMBus is a single-ended simple two-wire bus, which is typically used for low-bandwidth communications.

The LPI2C has the following key features:

- Standard, Fast, Fast+ and Ultra Fast modes
- High-speed mode (HS) in target mode
- Multi-controller, including synchronization and arbitration. Multi-controller means that any number of controller nodes can be present. Additionally, controller and target roles may be changed between messages (after a STOP is sent).
- Clock stretching. Sometimes multiple I2C nodes may drive the lines at the same time. If any I2C node is driving a line low, then that line is low. I2C nodes that are starting to transmit a logical one (by letting the line float high) can detect that the line is low. In this way, the nodes can identify that another I2C node is active at the same time.
    - When node detection is used on the SCL line, it is called clock stretching. Clock stretching is used as an I2C flow control mechanism.
    - When node detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one I2C node transmitter at a time.
- General call, seven-bit addressing, and ten-bit addressing
- Software reset, START byte, and Device ID (also require software support)

8.15.1 LPI2C1 Signals

Table 46: LPI2C1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
92		i2c1.SCL	0		SOC.C20
90		i2c1.SDA	0		SOC.C21

8.15.2 LPI2C2 Signals

Table 47: LPI2C2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
196	No AC	i2c2.SCL	0		SOC.D20
197	No AC	i2c2.SDA	0		SOC.D21

8.15.3 LPI2C3 Signals

LPI2C3 interface is used internally for accessing EEPROM, Codec, and PMIC chips.
This interface cannot be used.

8.15.4 LPI2C4 Signals

Table 48: LPI2C4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
43		i2c4.SCL	1		SOC.K21
45		i2c4.SDA	1		SOC.K20

8.15.5 LPI2C5 Signals

Table 49: LPI2C5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		i2c5.SCL	6		SOC.J20
88		i2c5.SCL	6		SOC.U20
39		i2c5.SDA	6		SOC.J21
87		i2c5.SDA	6		SOC.U18

8.15.6 LPI2C6 Signals

Table 50: LPI2C6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
43		i2c6.SCL	6		SOC.K21
115		i2c6.SCL	6		SOC.L18
45		i2c6.SDA	6		SOC.K20
171		i2c6.SDA	6		SOC.L17

8.15.7 LPI2C7 Signals

Table 51: LPI2C7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
174		i2c7.SCL	6		SOC.L21
175		i2c7.SCL	6		SOC.M21
124		i2c7.SDA	6		SOC.M20
176		i2c7.SDA	6		SOC.L20

8.15.8 LPI2C8 Signals

Table 52: LPI2C8 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
77		i2c8.SCL	6		SOC.N18
193	No TP	i2c8.SCL	6		SOC.N21
48		i2c8.SDA	6		SOC.N17
191	No TP	i2c8.SDA	6		SOC.N20

8.16 I3C - Improved Inter-Integrated Circuit

The MIPI Alliance Improved Inter-Integrated Circuit (MIPI I3C) improves upon the use and power of I2C, and provides an alternative to SPI for mid-speed applications.
The I3C bus protocol supports:

- In-band interrupts (IBI). These interrupts go from target to controller without extra wires, and the controller knows which target sent the interrupt.
- Common Command Codes (CCC)
- Dynamic addressing
- Multi-controller/multi-drop
- Hot-Join (HJ)
- I2C compatibility

The I3C peripheral supports all required and most optional features of the MIPI Alliance Specification for I3C, v1.0 and v1.1, except for ternary data rates (HDR-TSP and HDR-TSL).

The I3C module has the following key features:

- Two-wire multi-drop bus capable of 12.5 MHz clock speeds, with up to 11 devices.
    - Uses standard pads with 4 mA drive.
    - Dynamically assigns target addresses, and targets do not require static addresses. However, targets may have an I2C static address assigned at start-up, so the target can operate on an I2C bus. By default, I3C supports seven-bit I2C-style addresses.
    - Supports extended I2C 10-bit addressing through Map Feature Control 1 (SMAPCTRL1) register.
    - Allows targets to use the inbound SCL clock as the peripheral clock (instead of the clock from the controller) so devices can have slow or inaccurate clocks internally.
    - Allows simple targets, such as temperature sensors, to have no internal clock.
    - I3C controller supports handoff from Open Drain to Push-Pull mode for ACK to data transfer.
    - Normally the controller terminates the read, but for I3C, the target can also end the read.
- In-Band Interrupts (IBI) allow targets to send notifications to a controller.
    - Can be equivalent to a separate GPIO, but can also be directly data-bearing.
    - Can be prioritized. When multiple targets send interrupts to a controller at the same time, the order is resolved. Dynamic addresses establish the priority of the targets, so the controller controls the priority of the targets. Targets with lower-value dynamic addresses are higher priority level IBIs.

- Can start interrupts even when the controller is not active on the bus. No free-running clock is needed, but starting an interrupt requires a Bus Available condition.
- Can resolve an initial event via a time-stamping option, not requiring an interrupt.

- Built-in commands are in a separate space. These commands do not collide with normal controller-to-target messages.
  - Controls bus behavior, modes and states, low-power state, inquiries, and more.
  - Has additional room for new built-in commands to be used by other groups.
- Organized forms of multi-controller modes:
  - Secondary controllers, which use clean handoffs between different controllers.
- Hot-join onto I3C bus allows devices to connect to the bus later than when the bus starts.
  - Enables a device or module to get onto the I3C bus when it woke up after power-up or was physically inserted onto the I3C bus.
  - Provides a clean method for notification when new devices or modules get onto the I3C bus.
- Can use both I2C and I3C buses.
  - I3C supports specific legacy I2C devices on the bus.
  - I3C target devices can operate on I2C buses.
  - Supports bridging to I2C, SPI, UART, and other buses.
- Higher data rate modes are available.
  - Has a High Data Rate - Double Data Rate (HDR-DDR) mode, which is double the data rate of SDR (about 20 Mbit/s)
  - Only the controller and the specific target must support the higher data rate. The other targets can ignore it.

The I3C peripheral supports the full I3C feature set, except for the ternary data rates (HDR-TSP and HDR-TSL).

8.16.1.1 I3C Signals

Table 53: I3C Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
196	No AC	i3c1.PUR	1		SOC.D20
196	No AC	i3c1.PUR_B	6		SOC.D20
92		i3c1.SCL	1		SOC.C20
90		i3c1.SDA	1		SOC.C21
9	No EC	i3c2.PUR	2	1.8V level signal	SOC.T12
64		i3c2.PUR	2	3.3V by default. Referenced to LDO5 voltage.	SOC.Y19
9	No EC	i3c2.PUR_B	6	1.8V level signal	SOC.T12
64		i3c2.PUR_B	3	3.3V by default. Referenced to LDO5 voltage.	SOC.Y19
74		i3c2.SCL	2	Goes through level translator	SOC.AA11
80		i3c2.SCL	2	3.3V by default. Referenced to LDO5 voltage.	SOC.Y17
30		i3c2.SDA	2	Goes through level translator	SOC.AA10
60		i3c2.SDA	2	3.3V by default. Referenced to LDO5 voltage.	SOC.AA19

8.17 GPIO - General-Purpose Input/Output

The VAR-SOM-MX93 exposes up to 87 General-Purpose Input/Output pins.

The GPIO module has the following key features:

- Port Data Input (PDIR) register displays the logic value on each pin when the pin is configured for any digital function provided the corresponding Port Control and Interrupt module for that pin are enabled.
- Port Data Output (PDOR) register with corresponding set/clear/toggle registers controls output data of each pin when the pin is configured for the GPIO function.
- Port Data Direction (PDDR) register controls the direction of each pin when the pin is configured for the GPIO function.
- Port Input Disable (PIDR) register controls the disable of the input for each general-purpose pin.
- Pin interrupts
    - Interrupt flag and enable registers for each pin are functional in all digital pin muxing modes.
    - Support for interrupt or DMA request configured per pin.
    - Support for edge sensitive (rising or falling, or both) or level sensitive (low, high) configured per pin.
    - Asynchronous wake-up in Low-Power modes.
    - GPIO module generates a total of 2 interrupts and 2 DMA requests.
    - Each pin can be used to generate a single interrupt or DMA request.
- Protection registers
    - Each pin is configured for Secure or Non-Secure and Privilege/Non-Privilege access.
    - Each interrupt and DMA request domain is configured for Secure or Non-Secure and Privilege/Non-Privilege access.

8.17.1.1 GPIO Signals

Table 54: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
92		gpio1.IO[0]	5		SOC.C20
90		gpio1.IO[1]	5		SOC.C21
196	No AC	gpio1.IO[2]	5		SOC.D20
197	No AC	gpio1.IO[3]	5		SOC.D21
83		gpio1.IO[4]	5		SOC.E20
85		gpio1.IO[5]	5		SOC.E21
20	No AC	gpio1.IO[6]	5		SOC.F20
44		gpio1.IO[8]	5		SOC.G17
46		gpio1.IO[9]	5		SOC.J17
72		gpio1.IO[10]	5		SOC.G18
199	No AC	gpio1.IO[11]	5		SOC.G21
200	No AC	gpio1.IO[12]	5		SOC.G20
18	No AC	gpio1.IO[13]	5		SOC.H21
198	No AC	gpio1.IO[14]	5		SOC.H20
39		gpio2.IO[0]	0		SOC.J21
41		gpio2.IO[1]	0		SOC.J20
45		gpio2.IO[2]	0		SOC.K20
43		gpio2.IO[3]	0		SOC.K21
171		gpio2.IO[4]	0		SOC.L17
115		gpio2.IO[5]	0		SOC.L18
176		gpio2.IO[6]	0		SOC.L20
174		gpio2.IO[7]	0		SOC.L21
124		gpio2.IO[8]	0		SOC.M20
175		gpio2.IO[9]	0		SOC.M21
77		gpio2.IO[11]	0		SOC.N18
191	No TP	gpio2.IO[12]	0		SOC.N20
193	No TP	gpio2.IO[13]	0		SOC.N21
187	No TP	gpio2.IO[14]	0		SOC.P20
189	No TP	gpio2.IO[15]	0		SOC.P21
25		gpio2.IO[16]	0		SOC.R21
86		gpio2.IO[17]	0		SOC.R20
22		gpio2.IO[18]	0		SOC.R18
23		gpio2.IO[19]	0		SOC.R17
21		gpio2.IO[20]	0		SOC.T20
26		gpio2.IO[21]	0		SOC.T21
87		gpio2.IO[22]	0		SOC.U18
88		gpio2.IO[23]	0		SOC.U20
17		gpio2.IO[24]	0		SOC.U21
68		gpio2.IO[25]	0		SOC.V21
24		gpio2.IO[26]	0		SOC.V20

Pin#	Assy	Pin Function	Alt#	Notes	Ball
69		gpio2.IO[27]	0		SOC.W21
80		gpio3.IO[0]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.Y17
60		gpio3.IO[1]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.AA19
64		gpio3.IO[2]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.Y19
62		gpio3.IO[3]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.Y18
63		gpio3.IO[4]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.AA18
61		gpio3.IO[5]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.Y20
65		gpio3.IO[6]	5	3.3V by default. Referenced to LDO5 voltage.	SOC.AA20
145	No WB or WBD	gpio3.IO[20]	5	1.8V level signal	SOC.V16
147	No WB or WBD	gpio3.IO[21]	5	1.8V level signal	SOC.U16
84	No WB or WBD	gpio3.IO[22]	5	1.8V level signal	SOC.T16
31	No WB or WBD	gpio3.IO[23]	5	1.8V level signal	SOC.V14
33	No WB or WBD	gpio3.IO[24]	5	1.8V level signal	SOC.U14
35	No WB or WBD	gpio3.IO[25]	5	1.8V level signal	SOC.T14
29		gpio3.IO[26]	5	1.8V level signal. Has an internal 12K pull down	SOC.AA2
40		gpio3.IO[27]	5	1.8V level signal	SOC.Y3
53		gpio3.IO[28]	5	1.8V level signal. Can be used if BT disabled	SOC.W1
50		gpio3.IO[29]	5	1.8V level signal. Can be used if BT disabled. Has an internal 10K pull down	SOC.W2
51		gpio3.IO[30]	5	1.8V level signal. Can be used if BT disabled	SOC.Y1
52		gpio3.IO[31]	5	1.8V level signal. Can be used if BT disabled	SOC.Y2
74		gpio4.IO[0]	5	Goes through level translator	SOC.AA11
30		gpio4.IO[1]	5	Goes through level translator	SOC.AA10
3	No EC	gpio4.IO[2]	5	1.8V level signal	SOC.V12
5	No EC	gpio4.IO[3]	5	1.8V level signal	SOC.U12
9	No EC	gpio4.IO[4]	5	1.8V level signal	SOC.T12
11	No EC	gpio4.IO[5]	5	1.8V level signal	SOC.W11
1	No EC	gpio4.IO[6]	5	1.8V level signal	SOC.V10
58	No EC	gpio4.IO[7]	5	1.8V level signal	SOC.U10
15	No EC	gpio4.IO[8]	5	1.8V level signal	SOC.Y8
16	No EC	gpio4.IO[9]	5	1.8V level signal	SOC.AA7
4	No EC	gpio4.IO[10]	5	1.8V level signal	SOC.AA8
6	No EC	gpio4.IO[11]	5	1.8V level signal	SOC.Y9
10	No EC	gpio4.IO[12]	5	1.8V level signal	SOC.AA9
12	No EC	gpio4.IO[13]	5	1.8V level signal	SOC.Y10
55		gpio4.IO[16]	5	1.8V level signal	SOC.T10
56		gpio4.IO[17]	5	1.8V level signal	SOC.V8
177		gpio4.IO[18]	5	1.8V level signal	SOC.U8
73		gpio4.IO[19]	5	1.8V level signal	SOC.T8
113		gpio4.IO[20]	5	1.8V level signal	SOC.V6
96		gpio4.IO[21]	5	1.8V level signal	SOC.U6
120		gpio4.IO[22]	5	1.8V level signal	SOC.Y4
57		gpio4.IO[23]	5	1.8V level signal	SOC.AA3

Pin#	Assy	Pin Function	Alt#	Notes	Ball
122		gpio4.IO[24]	5	1.8V level signal	SOC.AA4
81		gpio4.IO[25]	5	1.8V level signal	SOC.Y5
71		gpio4.IO[26]	5	1.8V level signal	SOC.AA5
54		gpio4.IO[27]	5	1.8V level signal	SOC.Y6
75		gpio4.IO[28]	5	1.8V level signal	SOC.U4

8.18 FlexIO - Flexible I/O

Flexible I/O (FlexIO) is a highly configurable module providing a wide range of functionality, including:

- Emulation of various serial or parallel communication protocols
- Flexible 16-bit timers with support for various trigger, reset, enable, and disable conditions
- Programmable logic blocks which allow the implementation of digital logic functions on-chip and configurable interaction of internal and external modules
- Programmable state machine for offloading basic system control functions from the CPU

The FlexIO module has the following key features:

- Array of 32-bit shift registers with transmit, receive, data match, logic, and state modes
- Double-buffered shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start and stop bit generation
- 1, 2, 4, 8, 16, or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA, or polled transmit and receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during Stop mode
- Highly flexible 16-bit timers with support for various internal or external trigger, reset, enable, and disable conditions
- Programmable logic mode for integrating external digital logic functions on-chip, or combining pin, shifter, or timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU, with support for up to eight states, eight outputs, and three selectable inputs per state
- Integrated general purpose input/output registers and pin rising or falling edge interrupts to simplify software support
- Support for a wide range of protocols, including but not limited to:
    - UART
    - I2C
    - SPI
    - I2S
    - Camera IF
    - Motorola 68K or Intel 8080 bus
    - PWM or waveform generation
    - Input-capture (pulse edge interval measurement), such as SENT

8.18.1 FlexIO Signals

Table 55: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
39		flexio1.FLEXIO[0]	7		SOC.J21
80		flexio1.FLEXIO[0]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.Y17
41		flexio1.FLEXIO[1]	7		SOC.J20
60		flexio1.FLEXIO[1]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.AA19
45		flexio1.FLEXIO[2]	7		SOC.K20
64		flexio1.FLEXIO[2]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.Y19
43		flexio1.FLEXIO[3]	7		SOC.K21
62		flexio1.FLEXIO[3]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.Y18
48		flexio1.FLEXIO[10]	7		SOC.N17
63		flexio1.FLEXIO[4]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.AA18
171		flexio1.FLEXIO[4]	7		SOC.L17
61		flexio1.FLEXIO[5]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.Y20
115		flexio1.FLEXIO[5]	7		SOC.L18
65		flexio1.FLEXIO[6]	4	3.3V by default. Referenced to LDO5 voltage.	SOC.AA20
176		flexio1.FLEXIO[6]	7		SOC.L20
174		flexio1.FLEXIO[7]	7		SOC.L21
124		flexio1.FLEXIO[8]	7		SOC.M20
175		flexio1.FLEXIO[9]	7		SOC.M21
77		flexio1.FLEXIO[11]	7		SOC.N18
193	No TP	flexio1.FLEXIO[13]	7		SOC.N21
187	No TP	flexio1.FLEXIO[14]	7		SOC.P20
189	No TP	flexio1.FLEXIO[15]	7		SOC.P21
25		flexio1.FLEXIO[16]	7		SOC.R21
86		flexio1.FLEXIO[17]	7		SOC.R20
22		flexio1.FLEXIO[18]	7		SOC.R18
21		flexio1.FLEXIO[20]	7		SOC.T20
145	No WB or WBD	flexio1.FLEXIO[20]	4	1.8V level signal	SOC.V16
147	No WB or WBD	flexio1.FLEXIO[21]	4	1.8V level signal	SOC.U16
84	No WB or WBD	flexio1.FLEXIO[22]	4	1.8V level signal	SOC.T16
87		flexio1.FLEXIO[22]	7		SOC.U18
31	No WB or WBD	flexio1.FLEXIO[23]	4	1.8V level signal	SOC.V14
88		flexio1.FLEXIO[23]	7		SOC.U20
17		flexio1.FLEXIO[24]	7		SOC.U21
33	No WB or WBD	flexio1.FLEXIO[24]	4	1.8V level signal	SOC.U14
35	No WB or WBD	flexio1.FLEXIO[25]	4	1.8V level signal	SOC.T14
68		flexio1.FLEXIO[25]	7		SOC.V21
29		flexio1.FLEXIO[26]	4	1.8V level signal. Has an internal 12K pull down	SOC.AA2
40		flexio1.FLEXIO[27]	4	1.8V level signal	SOC.Y3
69		flexio1.FLEXIO[27]	7		SOC.W21

Pin#	Assy	Pin Function	Alt#	Notes	Ball
51		flexio1.FLEXIO[30]	4	1.8V level signal. Can be used if BT disabled	SOC.Y1
52		flexio1.FLEXIO[31]	4	1.8V level signal. Can be used if BT disabled	SOC.Y2
74		flexio2.FLEXIO[0]	4	Goes through level translator	SOC.AA11
30		flexio2.FLEXIO[1]	4	Goes through level translator	SOC.AA10
3	No EC	flexio2.FLEXIO[2]	4	1.8V level signal	SOC.V12
5	No EC	flexio2.FLEXIO[3]	4	1.8V level signal	SOC.U12
9	No EC	flexio2.FLEXIO[4]	4	1.8V level signal	SOC.T12
11	No EC	flexio2.FLEXIO[5]	4	1.8V level signal	SOC.W11
1	No EC	flexio2.FLEXIO[6]	4	1.8V level signal	SOC.V10
58	No EC	flexio2.FLEXIO[7]	4	1.8V level signal	SOC.U10
15	No EC	flexio2.FLEXIO[8]	4	1.8V level signal	SOC.Y8
16	No EC	flexio2.FLEXIO[9]	4	1.8V level signal	SOC.AA7
4	No EC	flexio2.FLEXIO[10]	4	1.8V level signal	SOC.AA8
6	No EC	flexio2.FLEXIO[11]	4	1.8V level signal	SOC.Y9
10	No EC	flexio2.FLEXIO[12]	4	1.8V level signal	SOC.AA9
12	No EC	flexio2.FLEXIO[13]	4	1.8V level signal	SOC.Y10
55		flexio2.FLEXIO[16]	4	1.8V level signal	SOC.T10
56		flexio2.FLEXIO[17]	4	1.8V level signal	SOC.V8
177		flexio2.FLEXIO[18]	4	1.8V level signal	SOC.U8
73		flexio2.FLEXIO[19]	4	1.8V level signal	SOC.T8
113		flexio2.FLEXIO[20]	4	1.8V level signal	SOC.V6
96		flexio2.FLEXIO[21]	4	1.8V level signal	SOC.U6
120		flexio2.FLEXIO[22]	4	1.8V level signal	SOC.Y4
57		flexio2.FLEXIO[23]	4	1.8V level signal	SOC.AA3
122		flexio2.FLEXIO[24]	4	1.8V level signal	SOC.AA4
81		flexio2.FLEXIO[25]	4	1.8V level signal	SOC.Y5
71		flexio2.FLEXIO[26]	4	1.8V level signal	SOC.AA5
54		flexio2.FLEXIO[27]	4	1.8V level signal	SOC.Y6
75		flexio2.FLEXIO[28]	4	1.8V level signal	SOC.U4
53		flexio2.FLEXIO[30]	4	1.8V level signal. Can be used if BT disabled	SOC.W1
50		flexio2.FLEXIO[31]	4	1.8V level signal. Can be used if BT disabled. Has an internal 10K pull down	SOC.W2

8.19 LPTMR - Low-Power Timer

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-power modes. It is reset only on Power on Reset (POR) or Low Voltage Detect (LVD), allowing it to be used as a time-of-day counter.

The LPTMR module has the following key features:

- 32-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wake-up from any low-power mode.
  - Hardware trigger output.
  - Counter supports free-running mode or reset on compare.
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

8.19.1 LPTMR Signals

Table 56: LPTMR Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
44		lptmr1.ALT1	4		SOC.G17
46		lptmr1.ALT2	4		SOC.J17
72		lptmr1.ALT3	4		SOC.G18
6	No EC	lptmr2.ALT1	3	1.8V level signal	SOC.Y9
65		lptmr2.ALT1	1	3.3V by default. Referenced to LDO5 voltage.	SOC.AA20
10	No EC	lptmr2.ALT2	3	1.8V level signal	SOC.AA9
12	No EC	lptmr2.ALT3	3	1.8V level signal	SOC.Y10

8.20 Reference Clocks

The VAR-SOM-MX93 exposes the clock outputs from the internal CCM module which can be used to clock external devices.

8.20.1 Clock Signals

Table 57: Clock Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
29		ccmsrcgpcmix.CLKO1	0	1.8V level signal. Has an internal 12K pull down	SOC.AA2
40		ccmsrcgpcmix.CLKO2	0	1.8V level signal	SOC.Y3
75		ccmsrcgpcmix.CLKO3	0	1.8V level signal	SOC.U4

8.21 ADC

The VAR-SOM-MX93 integrates 1 ADC. The main features are:

- It includes eight channels, four of them connected to pins in the package.
- Support the 1MS/s frequency of operation
- Multiple modes of starting conversion (Normal, Injected)
- Normal mode supports One-Shot and Scan (continuous) conversions
- Injected mode supports One-Shot conversions only
- Support TRGMUX to allow 16 trigger channels to be used by any ADC channel

8.21.1 ADC Signals

Table 58: ADC Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
146		anamix.adc_in0	0	1.8V level signal	SOC.B19
148		anamix.adc_in1	0	1.8V level signal	SOC.A20
150		anamix.adc_in2	0	1.8V level signal	SOC.B20
151		anamix.adc_in3	0	1.8V level signal	SOC.B21

8.22 DAP - Debug Access Port

DAP is a standard Arm component, comprising of several components. These components are used to access the DAP from an external debugger and Access Ports to access on-chip debug system resources. The DAP supports 1149.1/Arm SW-DP interface, which means that the JTAG interface can be operate in standard 5-pin JTAG-DP interface or in 2-pin SW-DP interface. The following figure shows the connectivity between the DAP and the pads.

8.22.1 DAP Signals

Table 59: DAP Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
51		dap.TCLK_SWCLK	0	1.8V level signal. Can be used if BT disabled	SOC.Y1
68		dap.TCLK_SWCLK	5		SOC.V21
24		dap.TDI	5		SOC.V20
53		dap.TDI	0	1.8V level signal. Can be used if BT disabled	SOC.W1
17		dap.TDO_TRACESWO	5		SOC.U21
52		dap.TDO_TRACESWO	0	1.8V level signal. Can be used if BT disabled	SOC.Y2
50		dap.TMS_SWDIO	0	1.8V level signal. Can be used if BT disabled. Has an internal 10K pull down	SOC.W2
69		dap.TMS_SWDIO	5		SOC.W21

8.23 Power

8.23.1 Power

Table 60: Power

Pin#	Assy	Pin Function	Alt#	Notes	Ball
32, 34, 103, 105, 107, 109, 111		VCC_SOM		SOM Power	VCC_SOM
104		USB2_VBUS	0	USB Host VBUS (5V) input	SOC.D12
106		USB1_VBUS	0	USB Host VBUS (5V) input	SOC.A11
49		SOM_3V3_PER		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_3V3_PER

8.23.2 Ground

Table 61: Digital Ground Pins

Pin#	Assy	Pin Function	Alt#	Notes	Ball
2, 7, 8, 13, 14, 19, 27, 28, 37, 47, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185		GND		Digital ground	GND
195	AGND			Audio ground	AGND

8.24 General System Control

8.24.1 General System Control Signals

Table 62: General System Control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
49		SOM_3V3_PER		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_3V3_PER
136		PMIC_NINT		1.8V level signal. No internal pull up.	PCA9451.13
143		ONOFF		1.8V level signal. Has an internal 100k Pull up.	A19
142		PMIC_ON_REQ		1.8V level signal. Has an internal 100k Pull down.	A17
140		PMIC_STBY_REQ		1.8V level signal. Has an internal 100k Pull down.	B18
154		TAMPER0		1.8V level signal	B16
156		TAMPER1		1.8V level signal	F14
131		WDOG_ANY		Used internally to connect to PMIC. Has an internal 100k Pull up	J18
98		SYS_nRST_3V3		SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset. By default cold reset is performed power cycling the PMIC rails. Can be programmed to perform warm reset instead.	

Note: *Users using SOM_3V3_PER as a supply power source, required to add 10uF to 20uF ceramic capacitor rated to > 6.3V.*

8.24.2 Boot configuration

The VAR-SOM-MX93 can be boot from the following sources:

- Internal source - eMMC Flash memory
- External source - SD Card

The BOOT_MODE pins determine the boot source. On the SOM, BOOT_MODE [3:0] pins are strapped internally by 10K PU/PD resistors.
Boot source selection is done via **Pin 42** of the SOM-DIMM 200 pin connector.

Table 63: BOOT_SEL signal SOM-DIMM 200 pin connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
42		BOOT_SEL		Controls internal OR external boot source; Internal signal pulled up to SOM_PER_3V3 using 10K resistor; 0=EXT. BOOT 1/Float=INT. BOOT	INT. LOGIC

9. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1 DSCM

The SOM can be ordered with the DSCM option.
In this configuration the DSI and LVDS interfaces are swapped in order to support DSI pins compatibility to other SOMs made by Variscite.

9.2 Ethernet PHY

The SOM can be ordered without Ethernet PHY chip assembled; it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
when not assembled, SoC balls are exported to SOM connector instead of Ethernet interface pins.

9.3 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

9.4 Single/Dual band Wi-Fi and BT/BLE combo

The SOM can be ordered without the Single or Dual band Wi-Fi and BT/BLE combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

9.5 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled. This allows reducing the overall cost of the product in case the Resistive Touch is not used.
when not assembled, SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

9.6 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.7 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 64: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VCC_SOM	-0.3	3.6	V	
USB_OTG1_VBUS, USB_OTG2_VBUS	-0.3	5.25	V	
Vin/Vout input/output voltage range (GPIO Type Pins)	-0.3	OVDD+0.3		OVDD is the I/O supply voltage
ESD damage immunity Human Body Model (HBM)	--	TBD		
ESD damage immunity Charge Device Model (CDM)	--	TBD		

10.2 Operating Conditions

Table 65: Operating Ranges

Pin #	Assembly	Min	Typ	Max	Unit
VCC_SOM	No VBT	3.25	3.3	3.45	V
VCC_SOM	VBT	3.35	3.7	5.5	V
USB_OTG1_VBUS/ USB_OTG2_VBUS		4.75	5	5.25	V

10.3 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the VAR-SOM-MX93 uses 3.3V LVCMOS levels, except the following interfaces: SD2, ENET_QOS, ENET1, HDMI, PCIe, USB, MIPI-DSI, MIPI-CSI, LVDS.

***USB/MIPI-DSI/MIPI-CSI/LVDS*:** Interfaces follow a different standard since they are high-speed signals.

uSDHC2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.
With other alternative function user can determine the voltage uSDHC2 IOs bank will be 1.8V or 3.3V using gpio3.IO[19].

ENET_QOS: interface available in case SOM is ordered **without "EC"** configuration. IOs voltage is 1/8V.

ENET1: IOs voltage is 1/8V.

10.4 Power Consumption

Table 66: VAR-SOM-MX93 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.36V	0.65A	2.184W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz (Dual Band Module)
Run	3.36V	0.42A	1.411W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Dual Band Module)
Run	3.36V	0.4A	1.344W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Single Band Module)
Run	3.36V	0.66A	2.218W	Linux up. Ethernet0, Ethernet1 running Iperf
Run	3.36V	0.37A	1.243W	Linux up. Ethernet0, Ethernet1, Wi-Fi module up
Run	3.36V	0.2A	0.672W	Linux up
Standby	3.36V	18mA	0.06W	Memory retention mode Dual Band WiFi *(Preliminary value measured on SOM running NXP Beta kernel release)*
Standby	3.36V	21mA	0.07W	Memory retention mode Single Band WiFI *(Preliminary value measured on SOM running NXP Beta kernel release)*
Off (RTC)	3.36V	0.2mA	0.672mW	All power rails are Off, only Internal SoC RTC is powered
Minimum Recommended Power Supply	3.36V	2A	6.72w	See note below

Note: *The Wi-Fi module needs a power source that can provide a peak current of 750 mA for around 20 milliseconds during transmitter calibration, even though its max continuous supply current is less than 320 mA.*
Module calibration occurs:

- *When the Module is initially powered up.*
- *The module is reset.*
- *When the radio is initialized.*
- *Every two minutes after the radio is initialized.*

11. Environmental Specifications

Table 67: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage Temperature Range	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
MTBF Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 5000 Khrs *	

Note: *Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.*

*Preliminary information

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-3.0-M2-B**

12.2 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-MX8 family:

Variscite PN: VHP-VS8M

DISCLAIMER:
Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

12.3 SOM Dimensions

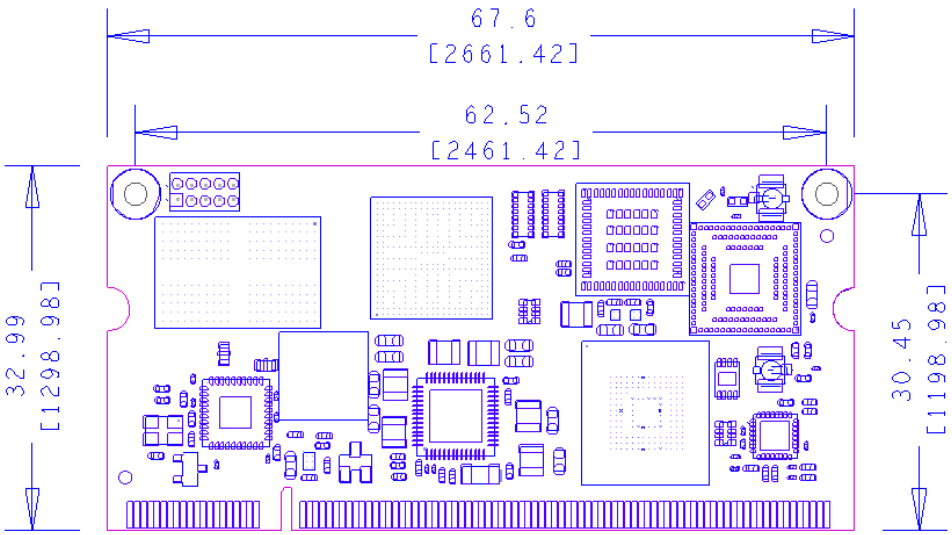


Figure 5: VAR-SOM-MX93 Mechanics in millimeters [mils]

12.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

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