For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

1. VAR-SOM-MX6
2. VAR-SOM-MX8
3. VAR-SOM-MXX
4. VAR-SOM-MX6MINI
5. VAR-SOM-MX6M-NANO
6. VAR-SOM-MX6M-PLUS
7. VAR-SOM-MX93
8. VAR-SOM-AM62

For complete alternate function per pin and specific SOM please refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at http://ftp.variscite.com/SOM_Compatibility
07. Camera, HDMI, DP

MIPI-CSI

Note:
MIPI-CSI#A signals appears on bottom side of J19 as of SymphonyBoard V1.4.

Switches and jumpers:
- J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):
Switch is to enable support for the following adapters:
- Parallel camera, HDMI, DisplayPort, etc.

MX8MP signals:
- MX8MP - via 50mbps buffer on SOM
- MX8MP - SOC IO

LVDS signals:
- MIPI-CSI-D3_P diff. pair for MX8MP
- MIPI-CSI-D3_N diff. pair for MX8MP

LAYOUT NOTE:
Base Per 3V3
Base Per 1V8
VCC_5V

Project:
Symphony-Board 1.6C_R1.23
Date: Monday, January 30, 2023
Approved By: Aviad H.
08. Ethernet

VDD_ENET for SOM-MX8/MX8X/MX8MP

Power for ENET1, PHY1 IOs on SOM power pin 21.38

For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY

LAYOUT NOTE:
Note: Customer requiring usage of J30 header (located on bottom side)

EXP_SOM_VSELECT

08. Ethernet (Internal)

LAYOUT NOTE:
Note: Customer requiring usage of J30 header (located on bottom side)

EXP_MDIO_EN

08. Ethernet (Internal)

LAYOUT NOTE:
Note: Customer requiring usage of J30 header (located on bottom side)

EXP_ENET1_RESET_B

LAYOUT NOTE:
Note: Customer requiring usage of J30 header (located on bottom side)
Note: 1. Default always ON, To disable clock install R21.
2. Replacement PN: AB-557-03-HCHC-F-L-C
3. Disabled with SW6 in ON state

Differential Impedance: 100 ohms

LAYOUT NOTE:
PCIE Differential Pairs, Follow PCIe routing guidelines.
Differential Impedance: 85 ohms Length match +/-5mil

1.5V_LDO Current limited to 300mA

PCIe CLK

LAYOUT NOTE:
Place parallel termination resistors close to the connector
R22, R23, R35, R36 assembled with Ferrite Bead P/N: BLM15BA330SN1D for EMI suppression

FOR SOM-MX6 using internal SoC clock:
install 100nF instead of R37, R38, remove R22, R23, R35, R36

mPCIexp

LAYOUT NOTE:
Place parallel termination resistors as close to the connector as possible.

Place AC caps close to the connector

PCIE Differential Pairs, Follow PCIe routing guidelines.
Differential Impedance: 85 ohms Length match +/-5mil

DSC5570344FL1T
10. Debug, GPIO Exp, Buttons, LED

**USB UART DEBUG**

![USB UART Debug Diagram]

**GPIO EXPANDER**

![GPIO Expander Diagram]

**GP BUTTON**

![GP Button Diagram]

**GP LED**

![GP LED Diagram]

**LAYOUT NOTE:**

USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines. Length Match: +/- 100 mils. Differential Impedance: 90 ohms.

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In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V. When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.
11. LVDS, DSI, Touch

RESISTIVE TOUCH

CAPACITIVE TOUCH

MIPI DSI DISPLAY

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression

Note for U30 U31: Recommended PN for new design FPF2193. Assembled board can have FPF2194.

Short circuit protection

See note in: "Headers" Page 14
12. USB2 Host

**USB2 Host**

**LAYOUT NOTE:**
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
Length Match: +/- 100 mils
Differential Impedance: 90 ohms

**NOTE:**
Power always enabled.
In order to control the power see page 14 "Headers"
USB TYPE C Circuitry

5V Source Load Switch

USB TYPE C

Config Channel Logic Detection & Indication of Plug Orientation
14. Headers

Headers arranged for compatible alternate function

- PWM#B
- UART#A
- UART#B

Headers arranged for partial compatible alternate function

- UART/QSPI
- SAI
- SPI#A
- I2C#B
- I2C#A
- CAN

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility

I2C#A has internal pulls in Camera buffer
I2C#B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Located on PS

SAI#A_RXFS_PCIE#A_RESET_B
SAI#A_RXD
SAI#A_TXD
SAI#A_TXFS

Symphony Board reset circuitry watch dog input

USB#A Host VBUS power control
In order to control the USB#A HOST VBUS power a short is required:

For all other watch dog looped on SOM

COLD RESET ON WDOG_B EVENT
for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility