## Revision History

<table>
<thead>
<tr>
<th>Document</th>
<th>Carrier</th>
<th>Issue</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1.0</td>
<td>Initial</td>
<td></td>
<td>Released</td>
</tr>
</tbody>
</table>
| 1.2      | 1.1     | Updated Block Diagram | Added SH1 wire short symbol  
Updated Compatibility values for SOM pins 68,69,176  
Updated Som pin 26 net name  
Fixed U28.B1, C113.1 net name  
Fixed R1.920.23 to 0 ohms |
| 1.3      | 1.2     | Removed SH1 wire short, 3.56 correct to capacitor touch  
Changed R93 to 0 ohms  
Changed R112 to 0 ohms  
Added Resistors R130-132  
Removed ADC_No alternate function from VAR-SOM-MX8 Symbol  
Updated PC18 resistor assembly  |
| 1.4      | 1.3     | Updated VAR-SOM-MX8M Symbol  
Fixed ETH pins on VAR-SOM-MX8 Symbol  |
| 1.5      | 1.2A    | Removed SH1 Wire  |
| 1.6      | 1.3     | Added VAR-SOM-MM MX8 Block Diagram and Symbol  
P/N RELEASE VERSION 1.1 Subject to change without notice  |
| 1.7      | 1.2B    | Added an extra USB  
Added an extra Ethernet  |
| 1.8      | 1.3     | Released  |
| 1.9      | 1.3     | Updated Block Diagram  
Updated the symbols for Som  
Updated the symbols for Som  
Fixed U22.B1, C113.1 net name  
Fixed R1.920.23 to 0 ohms |
| 1.10     | 1.3     | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.11     | 1.3     | Updated Block Diagram  
Added Resistors R130-132  
Changed the symbols for Som  
Updated the symbols for Som  
Fixed R1.920.23 to 0 ohms  
Fixed ETH pin names VAR-SOM-MX8X Symbol  
Updated Parallel Camera/HDMI/DP Note  |
| 1.12     | 1.3A    | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.13     | 1.4     | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.14     | 1.4A    | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.15     | 1.4A    | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.16     | 1.5     | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.17     | 1.5     | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.18     | 1.5     | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.19     | 1.6A    | Added SH1 wire short symbol  
Updated Som pin 26 net name  
Fixed R1-R2, R35-R38 net name  
Changed R123, R127 to N.C.  
Removed SH1 wire short, J1.68 routed to capacitive touch  |
| 1.20     | 1.6     | Ethernet PHY replaced to ADIN1300  
R22, R23, R56 assembly with Ferrule Base  
C185 assembled with 12K resistor, R20 not assembled  
U2 changed to CBT1.02043B  
USB3 crossover switch changed to CBT1.02043B  |
| 1.21     | 1.7     | Due to EOL, U23 changed to NFP1.1812TH1030D  
Due to allocation problems: U23 changed to 2N4058V/203203DE  |

### Disclaimer:

Schematics are for reference only. Variscite LTD provides no warranty for the use of these schematics. Schematics are subject to change without notice.
05. Power, Reset, Boot, RTC, EEPROM

POWER DISCHARGE

SOM BOOTSTRP

Boot Options:
OFF : INT
ON : SD
Internal boot is from eMMC
For supporting MX6 eMMC boot option:
Remove R93, Assembly R56,R11
Note: Normal configuration is with NAND
Note for U29: Recommended PN for new design FPF2193
Assembled board can have FPF2194.

12VDC INPUT
Main Switch

5V/8A FROM PWR JACK

3.35V/8A FROM PWR JACK

1.5V BASE

1.8V BASE

BASE_3V3

RTC BATTERY

RESET CIRCUITRY

FAN PWR

Variscite

Title Size Document Number Rev

Project

Approved By: Designer:

Address 0x5A,0x5B

05. Power,Reset,Boot,RTC,EEPROM

Date: Sheet

3 24 Monday, April 04, 2022

05. Power,Reset,Boot,RTC,EEPROM

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08. Ethernet

VDD_ENET for SOM-MX8/MX8X/MX8MP

Power for ENET1, RGMII IDs on SOM power feed from pin J1.36
For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY
Note: 1. Default always ON. To disable clock install R21.
2. Replacement PN: AB-557-03-HCHC-F-L-C-T
3. Disabled with SW6 in ON state

Differential Impedance: 100 ohms

PCIE_CLK

LAYOUT NOTE:
PCIE Differential Pairs. Follow PCIe routing guidelines. Differential Impedance: 85 ohms
Length match +/-5mil
10. Debug, GPIO Exp, Buttons, LED

**USB UART DEBUG**

- **BASE_PER_3V3**
- **3V3OUT**
- **DEBUG_VBUS**
- **U24 FT232QX**
- **C133 100μF**
- **U23 SN74AVC4245**
- **VBCC VBCC**
- **2DR 2DEP**
- **1A2 1B2**
- **2A1 2B1**
- **GND GND**

**LAYOUT NOTE:**
- USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
- Length Match: +/- 100 mils
- Differential Impedance: 90 ohms

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**GPIO EXPANDER**

- **BASE_PER_3V3**
- **I2C A SDA**
- **I2C A_SCL**
- **EXP_INT**
- **C135 100μF**
- **R19 10K**
- **VBCC VBCC**
- **P1 P2**
- **P3 P4**
- **P5 P6**
- **P7 P8**
- **P9 P10**
- **P11 P12**
- **GND GND**

**I2C ADDRESS: 0x20**

Powerup all IN
DM can set to output as push-pull

In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V. When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

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**GP BUTTON**

- **EXP_SW1**
- **EXP_SW2**
- **EXP_SW3**
- **SW1**
- **SW2**
- **SW3**

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**GP LED**

- **EXP_LED**

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**Variscite**

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**Title:** Symphony-Board 1.6A_R1.21

**Document Number:** A4

**Rev:** 1.6A_A_01

**Date:** Monday, April 04, 2022

**Sheet:** 8 of 24
11. LVDS, DSI, Touch

RESISTIVE TOUCH

CAPACITIVE TOUCH

LVDS DISPLAY A

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

LVDS DISPLAY B

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

MIPI DSI DISPLAY

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

Short circuit protection

See note in: "Headers" Page 14
12. USB2 Host

USB2 Host

LAYOUT NOTE:
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines.
Length Match: +/- 100 mils
Differential Impedance: 90 ohms

NOTE:
Power always enabled. In order to control the power see page 14 "Headers".
13. USB3, uSATA

SATA/USB select

LAYOUT NOTE:
USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

USB Profile 1 = 5 V @ 2.1 A

Config Channel Logic Detection & Indication of Plug Orientation

USB TYPE C Circuitry

5V Source Load Switch

LAYOUT NOTE:
USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

USB C_OTG_ID can be left floating if not used. For simple OTG function for VAR-SOM-MX8M-PLUS

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

Usage of native USB_ID for EMMC requires patches not included in the formal release, pull up should be 1.8V.

Connect J1.72 GP10 to U22 PIN 10 output

same solution applies also for VAR-SOM-MX8X/8M-MINI

USB#B_OTG_ID can be left floating if not used.

SATA 2.0
14. Headers

Headers arranged for compatible alternate function

- PWM#B
- UART#A
- UART#B
- BT UART

<table>
<thead>
<tr>
<th>J18</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
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<tbody>
<tr>
<td>PWMC</td>
<td>1</td>
<td>2</td>
<td>PWMC</td>
<td>1</td>
<td>2</td>
<td>PWMC</td>
<td>1</td>
<td>2</td>
<td>PWMC</td>
<td>1</td>
</tr>
<tr>
<td>UARTB_TX</td>
<td>3</td>
<td>4</td>
<td>UARTB_RX</td>
<td>5</td>
<td>6</td>
<td>UARTB_TX</td>
<td>7</td>
<td>8</td>
<td>UARTB_RX</td>
<td>9</td>
</tr>
<tr>
<td>UARTBT_CTL_B</td>
<td>10</td>
<td>11</td>
<td>UARTBT_CTL_B</td>
<td>12</td>
<td>13</td>
<td>UARTBT_CTL_B</td>
<td>14</td>
<td>15</td>
<td>UARTBT_CTL_B</td>
<td>16</td>
</tr>
</tbody>
</table>

I2C A has internal pulls in Camera buffer.
I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function

- UART/QSPI
- SAI/SPI

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS " located at: ftp://ftp.variscite.com/SOM_Compatibility

COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs
Listed above SOMs require short on headers to get "reboot" to function.
For all other watch dog looped on SOM

USB#A Host VBUS power control
In order to control the USB#A HOST VBUS power a short is required:
- Symphony Board reset: See J3.17
- Symphony Board power input: See J3.11
- MX6/SOLO: FIN3 NDSGL_B: See J13.1
- Symphony Board U2: See J3.12
- Control input: See J3.18
