# VAR-DT8MCustomBoard

Variscite

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## Disclaimer:


SchematicS are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.


## Revision History

| Document | Carrier | Description |
|---|---|---|
| 1.0 | 1.0 | INITIAL |
| 1.1 | 1.1 | 1st Release |
| 1.2 | 1.2 | Schottky_SSMINI - Replace symbol (swapped pin 1 and 2 to match silk) e.g. D1<br>DART_J1.31 - Update connector for NVCC_ENET pin<br>R110 - Assemble for PMIC_ON_REQ to go low for >130ms<br>BASE_PER_3V8 - feedback taken from SOM_VBAT (close to SOM) -Rev1.1. add on wire<br>R159 and R156 - Remove to allow FPF2193 auto restart<br>R176 - Replaced to 17.8K to allow for 5.4V power supply<br>C157 - Added on input power eFUSE - filter glitches<br>R65 - Remove - Part of boot config - not required.<br>Open Solder mask and add thermal pad under SOM |
| 1.3 | 1.3 | Added support for Basler MIPI-CSI camera<br>DP - Align with NXP reference design<br>DART-MX8M-MINI notes/block diagram and symbol added.<br>Added CAN-FD to SPI bridge circuitry |
| 1.4 | 1.3A | Limit DMIC_DATA to 1.8V swing using a voltage divider<br>Overdriving DMIC_DATA (>1.8V) (applicable only when recording DMIC input) will generate noise on Headphone output. |
| 1.5 | 1.3B | Added DisplayPort connector J20 and remove disclaimer note |
| 1.6 | 1.4 | Fix Layout for DMIC_DATA voltage divider<br>Add page 13. to Content list |
| 1.7 | 1.4 | Correct DART-MX8M and DART-MX8M-MINI J2 symbols for pin names on J2.2 and J2.14; See Pinmux changes for HPLOUT & DMIC_CLK nets. |
| 1.8 | 1.4A | Modify U44 MCP2517FDT CAN-FD controller to MCP2518FDT due to previous NRND<br>Added assembly note on page 13 |
| 1.9 | 1.4B | * C67 C76 updated - USB HUB Crystal capacitors<br>* C181 C182 updated CAN BUS Crytal capacitors<br>* PCIe RX caps replaced with 0 ohm resistors<br>* Update manufacturer PN for: U33 Q2 Q6<br>* Added U33 manufacturer PN status note. |
| 2.0 | 1.4C | * DART-MX8MP Block Diagram & Connectors added<br>* HDMI AC coupling and level termination modified to fit iMX8M-Plus<br>- Note added on HDMI/DP page<br>* Add note in DART-MX8MP Connector page for:<br>- SAI1 and SAI5 pads voltage level<br>- PMIC_ON_REQ<br>* Add note for DART-MX8MP USB1_ID and USB2_ID usage in page 8.<br>* Add note for Reset Button functionality with DART-MX8M-PLUS-V1.0A engineering samples in page 9.<br>* Add note for DART-MX8MP boot configuration on page 11. |

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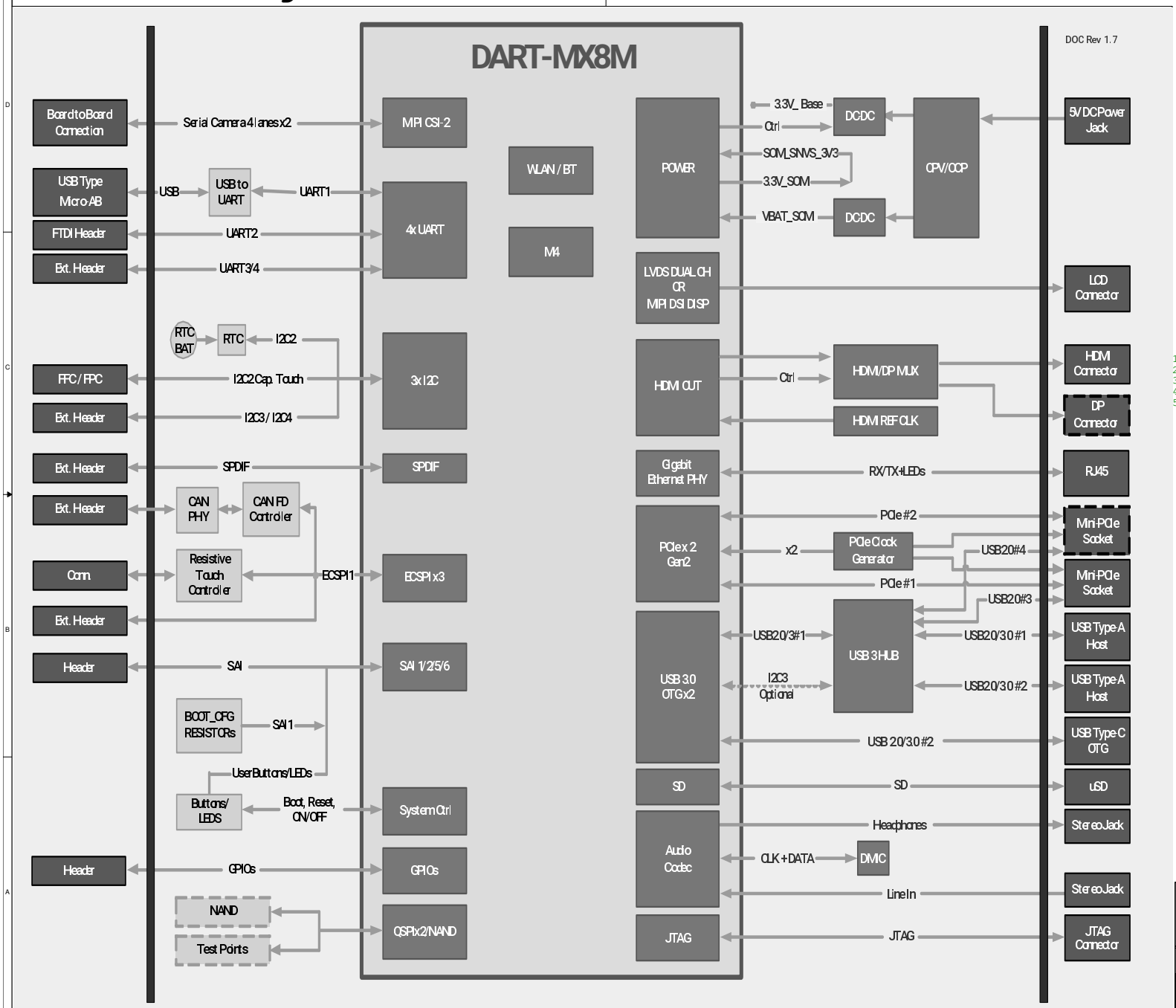
| | | | |
|---|---|---|---|
| Title: 01. Cover | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Thursday, November 19, 2020 | | Sheet 1 of 17 | |

# 02A. Block Diagram – DART-MX8M




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x60 SOM - Int. power ctrl.
0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P2 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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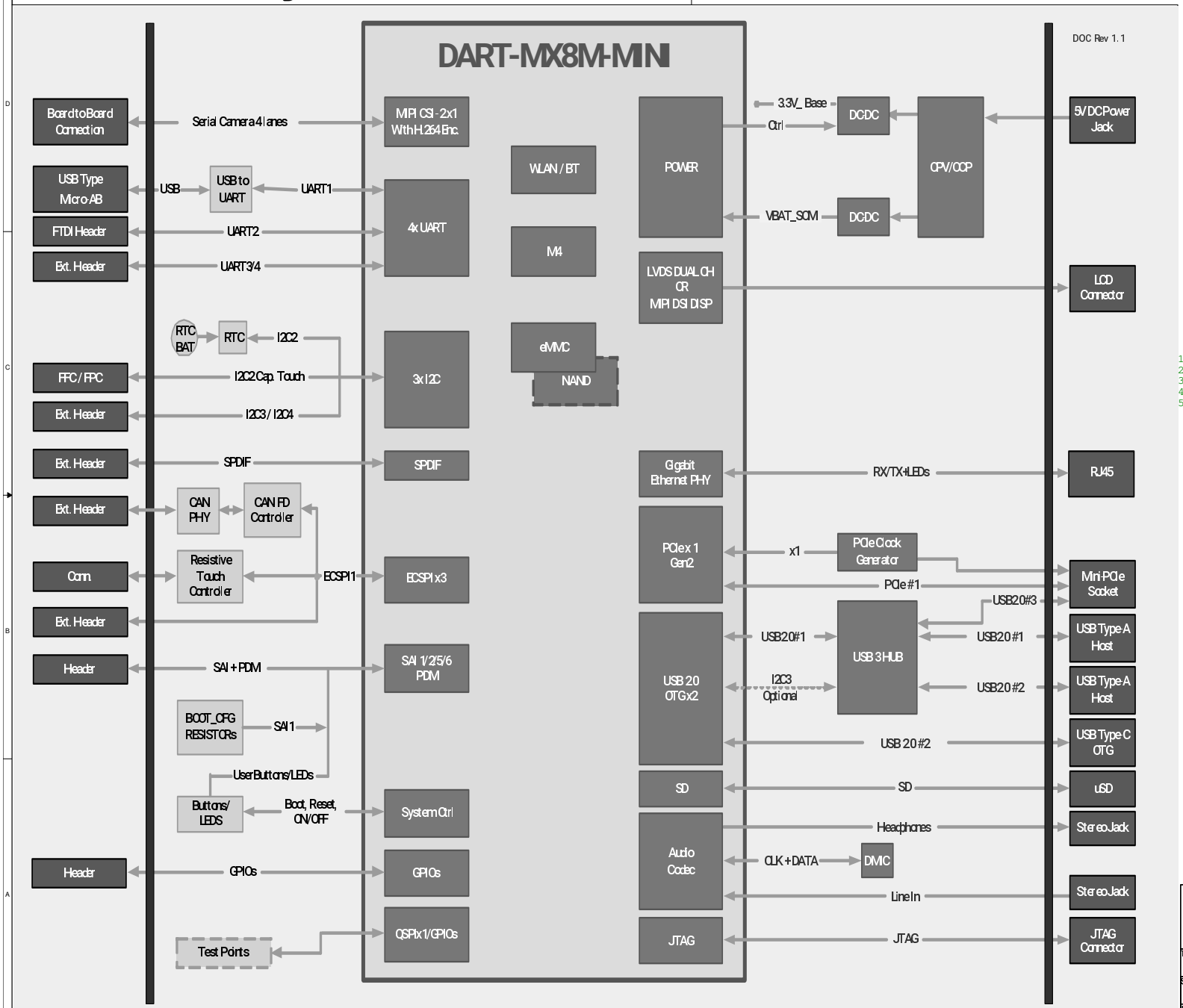
| | | | |
|---|---|---|---|
| Title: 02A. Block Diagram with DART-MX8M | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 2 of 17 | |

# 02B. Block Diagram – DART-MX8M-MINI




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU - 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU - 5K on SOM
0x1A SOM - Int. CODEC
0x2D USB3 HUB
0xXX Header J12

I2C4: PU - 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

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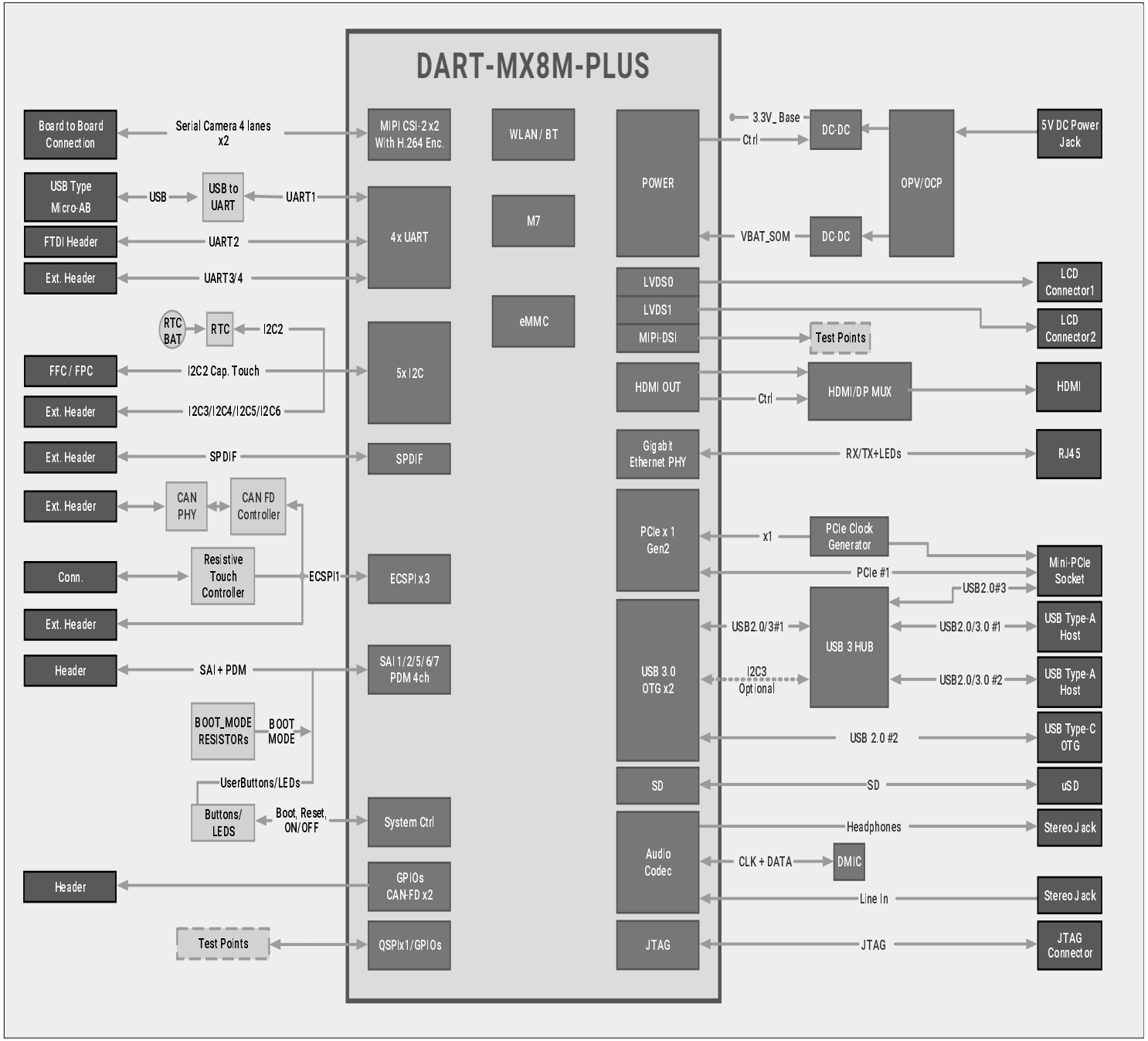
| | | | |
|---|---|---|---|
| Title: 02B. Block Diagram with DART-MX8M-MINI | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 3 of 17 | |

# 02C. Block Diagram – DART-MX8M-PLUS




**I2C BUS ADDRESS:**

I2C1: Internal to SOM

I2C2: PU – 10K on U8
10K on custom
0x54 BOARD ID EEPROM Page0
0x55 BOARD ID EEPROM Page1
0x68 RTC
0x38 CAPACITIVE TOUCH CTRLR
0x3D USB-C CC Logic PTN5150AHXMP
0x3C CSI P1 Camera (1V8) OV5640

I2C3: PU – 5K on SOM

0x2D USB3 HUB
0xXX Header J12

I2C4: PU – 10K on U8
10K on custom
0x3C CSI P1 Camera (1V8) OV5640
0xXX Header J12
0xXX mPCIe J23 & J32

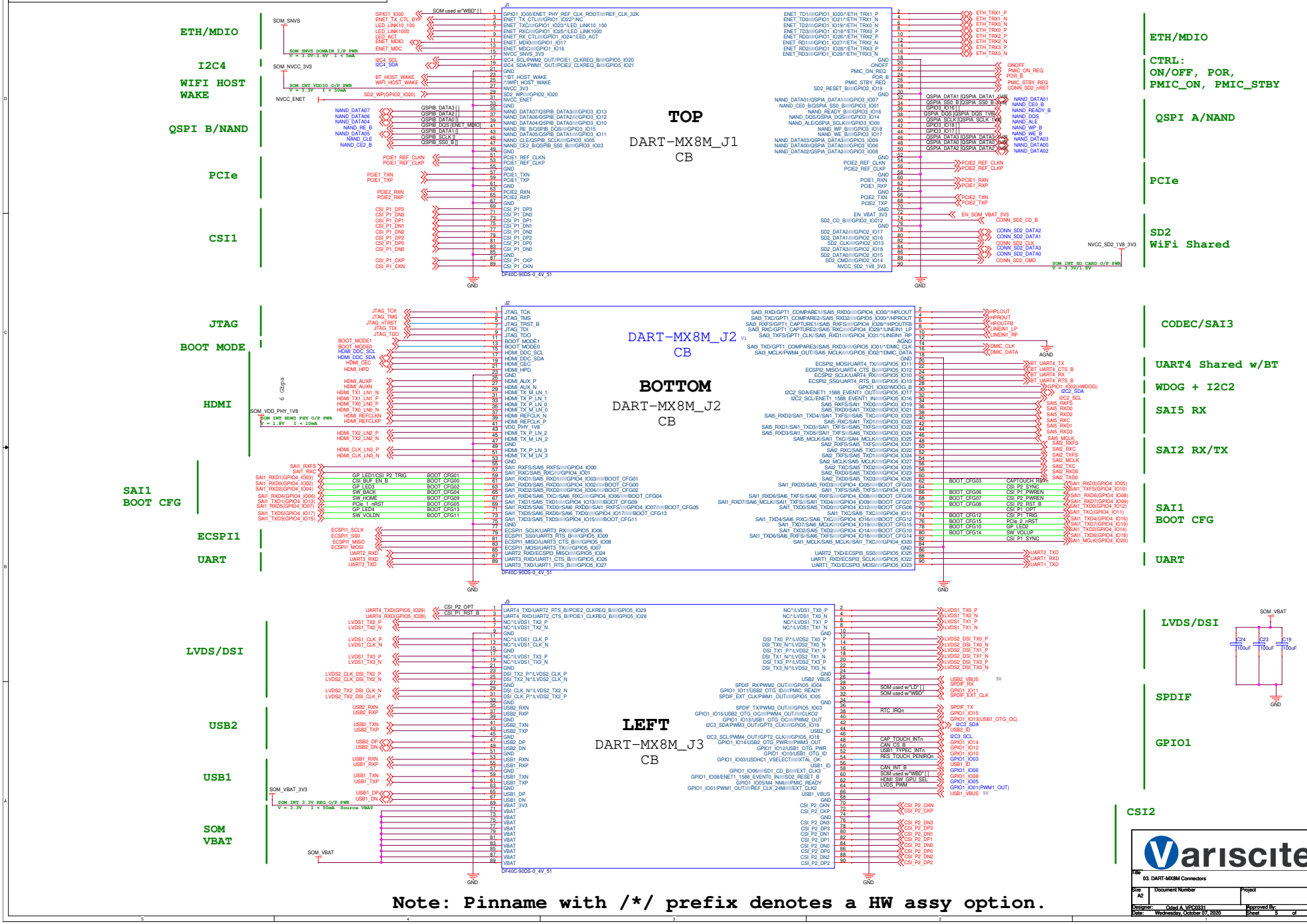
## Important Notes:

1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm

Variscite

| | | | |
|---|---|---|---|
| Title: 02B. Block Diagram with DART-MX8M-MINI | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 4 of 17 | |

# 03A – DART-MX8M Connectors



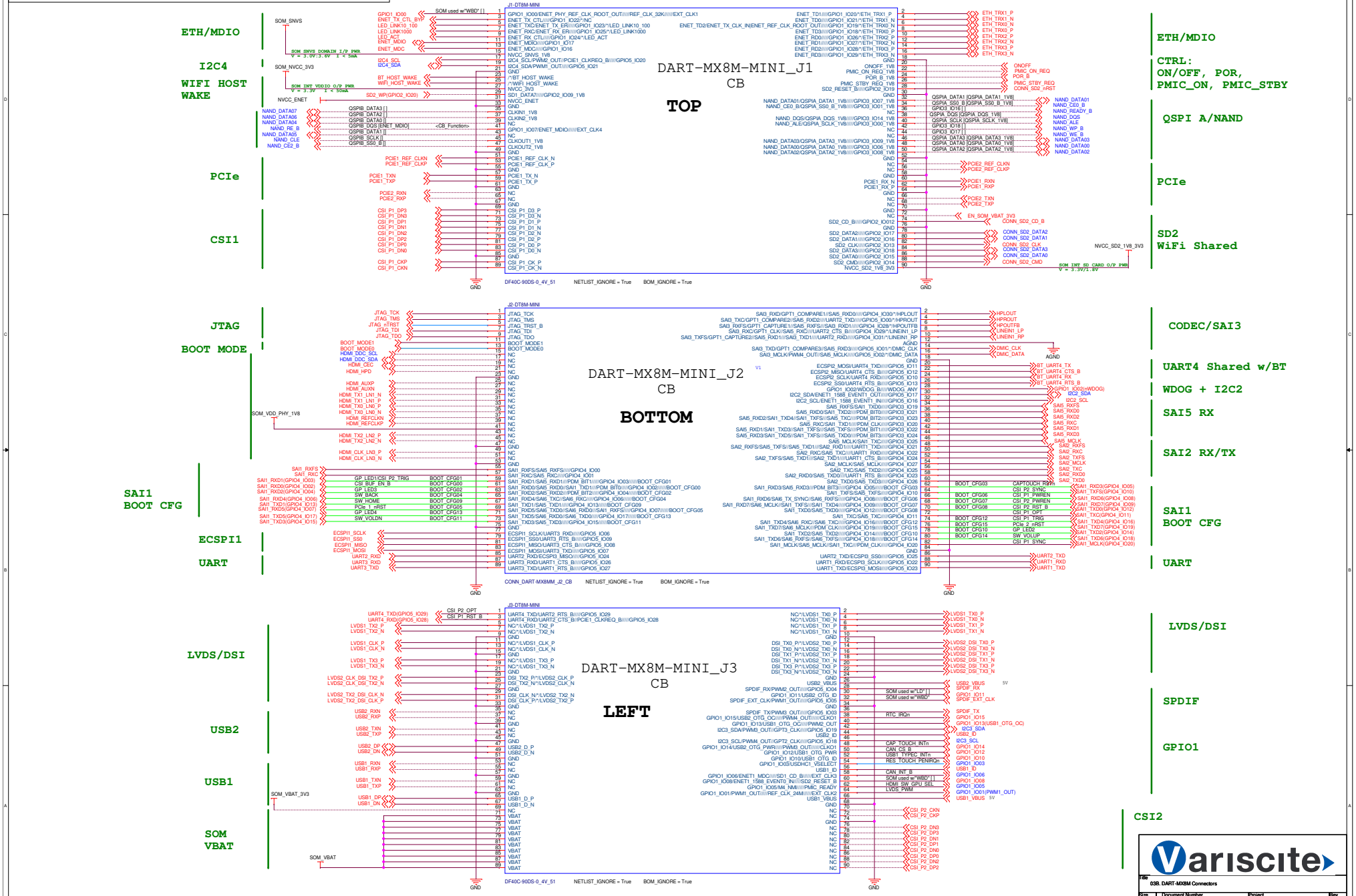

Note: Pinname with /*/ prefix denotes a HW assy option.

Variscite

| | | | |
|---|---|---|---|
| Title: 03. DART-MX8M Connectors | | | |
| Size: A2 | Document Number | Project | Rev: I.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 5 of 17 | |

# 03B – DART-MX8M-MINI Connectors

*** Dotted nets – Functionality differ from DART-MX8M. ***



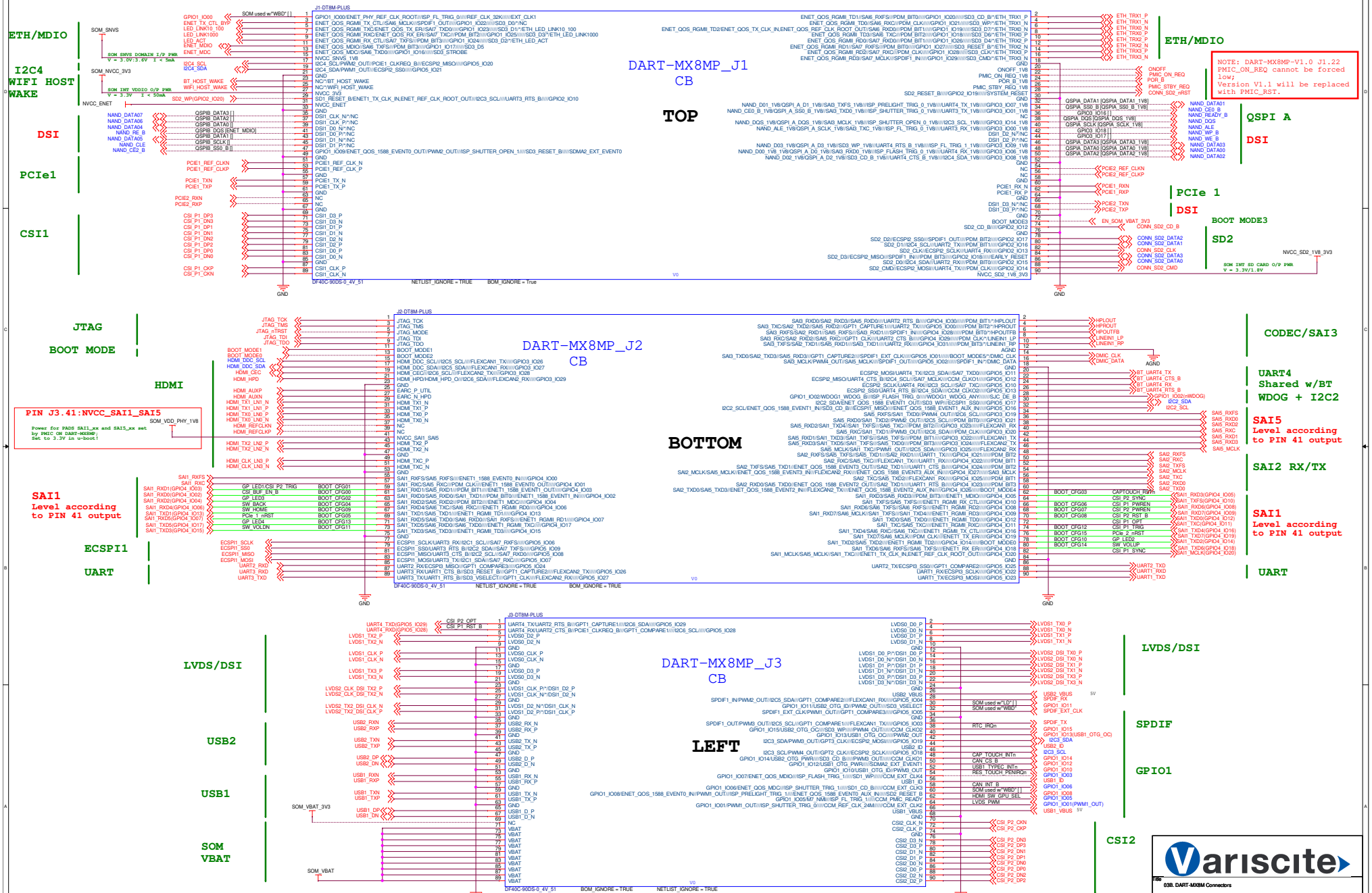

**Note: Pinname with /*/ prefix denotes a HW assy option.**

Variscite

| | |
|---|---|
| Title | 03B. DART-MX8M Connectors |
| Size | A2 |
| Document Number | |
| Project | |
| Rev | 1.4C-R2.0 |
| Designer: | Oded A. VPC0331 |
| Approved By: | |
| Date: | Wednesday, October 07, 2020 |
| Sheet | 6 of 17 |

# 03C – DART-MX8M-PLUS Connectors

*** Dotted nets – Functionality differ from DART-MX8M. ***

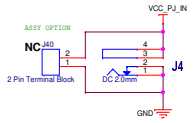



Note: Pinname with /*/ prefix denotes a HW assy option.

| | |
|---|---|
| Title | 03B. DART-MX8M Connectors |
| Size | A2 |
| Document Number | |
| Project | |
| Rev | 1.4C-R2.0 |
| Designer: | Oded A. VPC/0331 |
| Approved By: | |
| Date: | Wednesday, October 07, 2020 |
| Sheet | 7 of 17 |

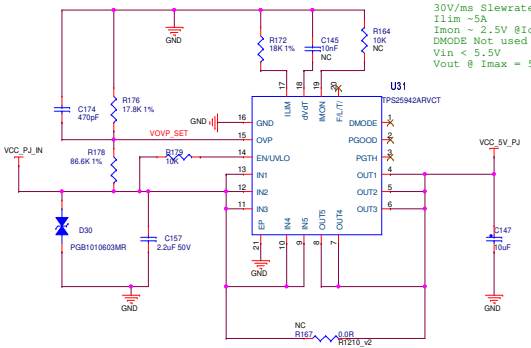
# 04. Power, RTC,Board ID

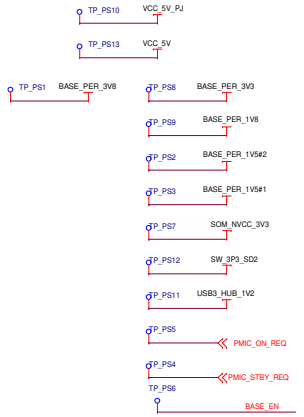
## 5VDC/4A POWER JACK



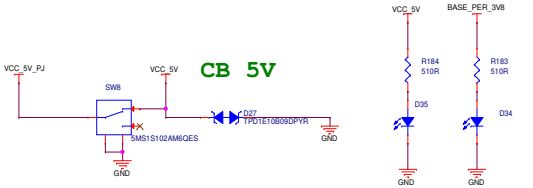

## PWR JACK 5V IN OVP/OCP

30V/ms Slewrate based on int. circuitry
Ilim ~5A
Imon ~ 2.5V @Iout=5A
DMODE Not used
Vin < 5.5V
Vout @ Imax = 5.2V

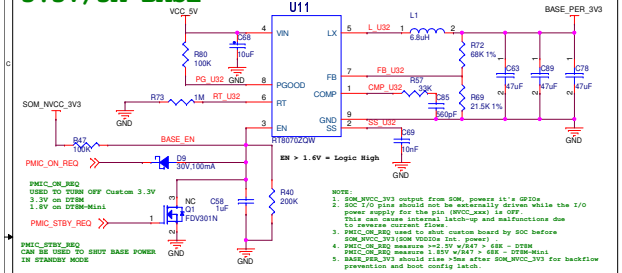


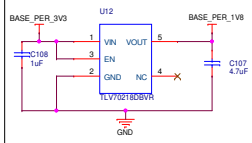

## POWER SW/(ON/OFF)



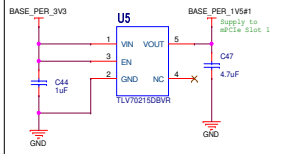

## 3.3V/3A BASE



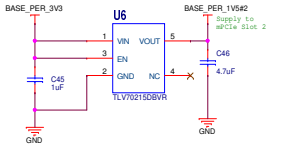

## 1.8V/0.3A BASE



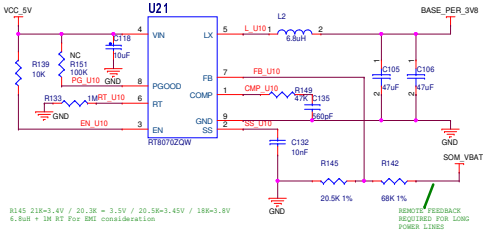

## 1.5V/0.3A #1 BASE



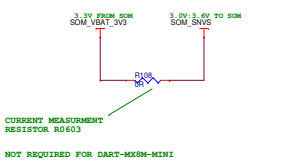

## 1.5V/0.3A #2 BASE



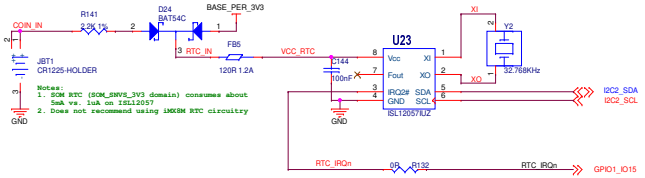

## 3.45V/3A FROM PWR JACK



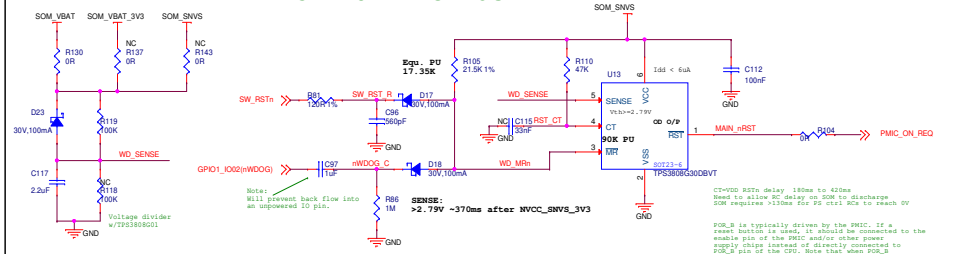

## SOM SNVS



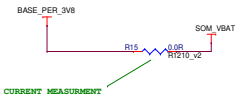

## RTC BATTERY



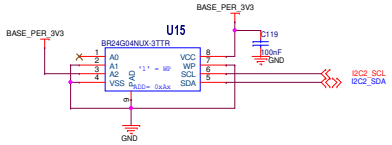

## RESET & WATCHDOG



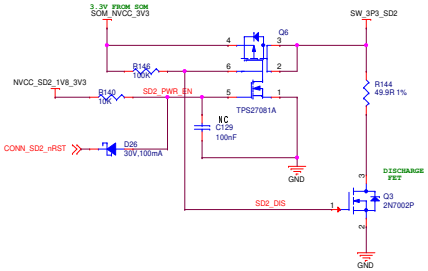

## SOM PWR



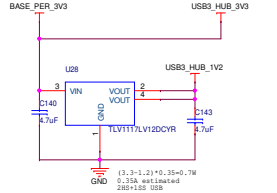

## BOARD ID



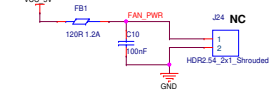

## SD POWER




## USB3 HUB POWER




## FAN : 5V/0.2A

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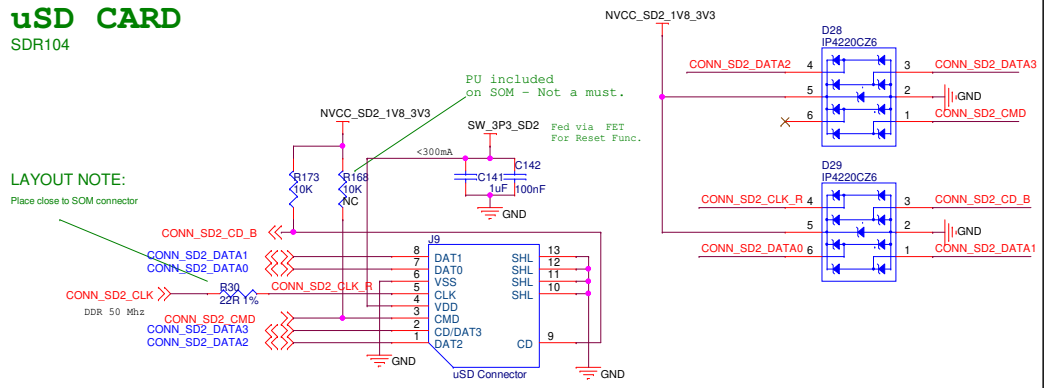
| | | | |
|---|---|---|---|
| Title: 04. Power, RTC,Board ID | | | |
| Size: A2 | Document Number | Project | Rev: 1.4C-R2.0 |
| Designer: Oded A. VRC0331 | | Approved By: | |
| Date: Thursday, October 08, 2020 | | Sheet 8 of 17 | |

# 05. ETH, uSD, AUDIO, MIPI-CSI

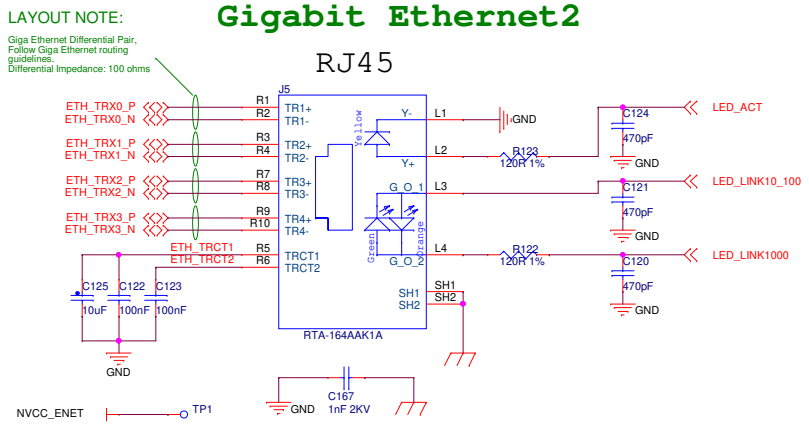
## uSD CARD

SDR104



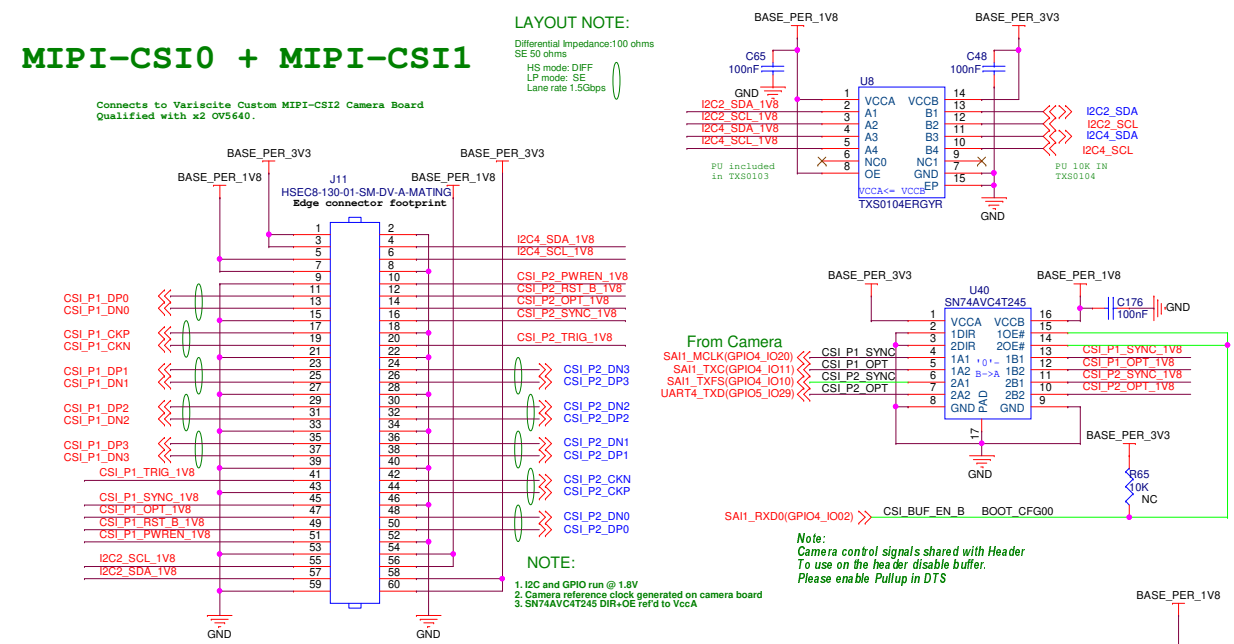

## Gigabit Ethernet2

RJ45



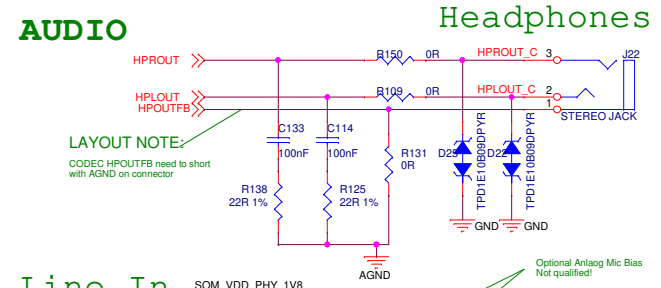

## MIPI-CSI0 + MIPI-CSI1

Connects to Variscite Custom MIPI-CSI2 Camera Board
Qualified with x2 OV5640.

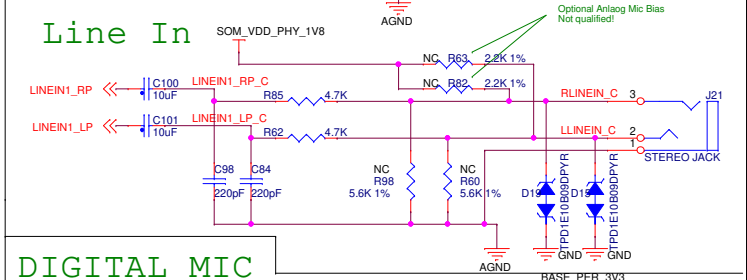



## AUDIO

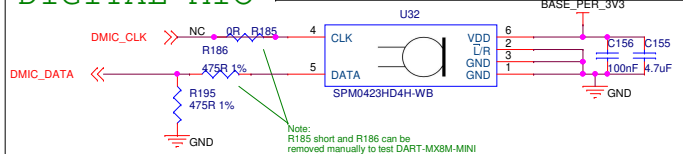
### Headphones




### Line In




### DIGITAL MIC



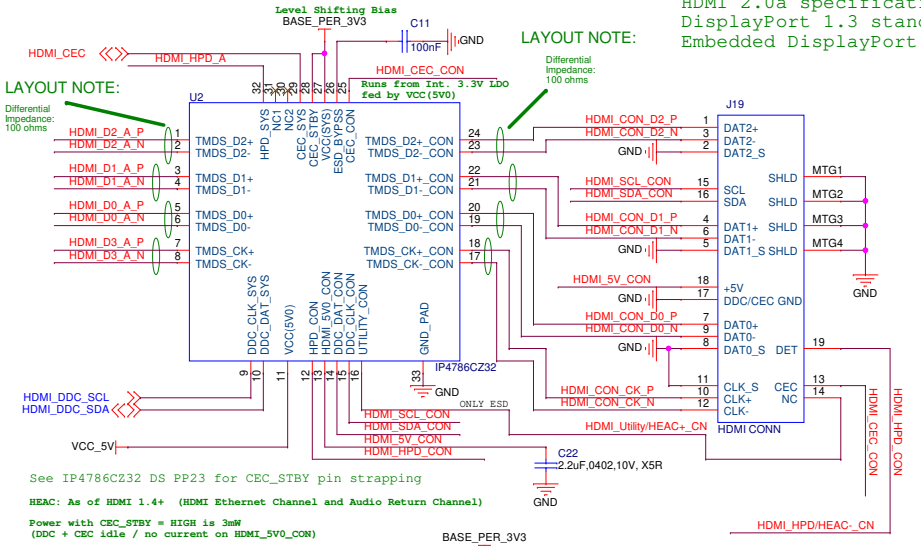

Variscite

| | | | |
|---|---|---|---|
| Title | 05. ETH, uSD, AUDIO, MIPI-CSI | | |
| Size A3 | Document Number VAR-DT8MCustomBoard | Project VAR-DT8MCustomBoard | Rev 1.4C-R2.0 |
| Designer: | Oded A. VPC0331 | Approved By: | |
| Date: | Wednesday, October 07, 2020 | Sheet 9 of 17 | |

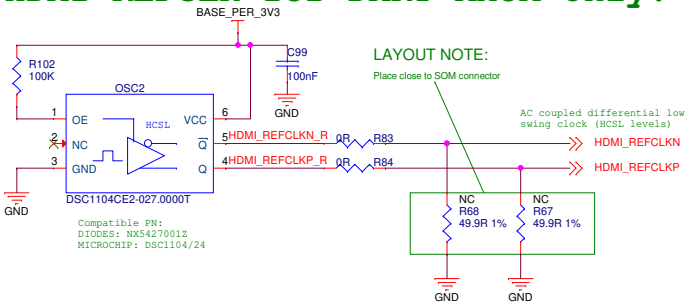
# 06. HDMI, eDP

## HDMI PORT

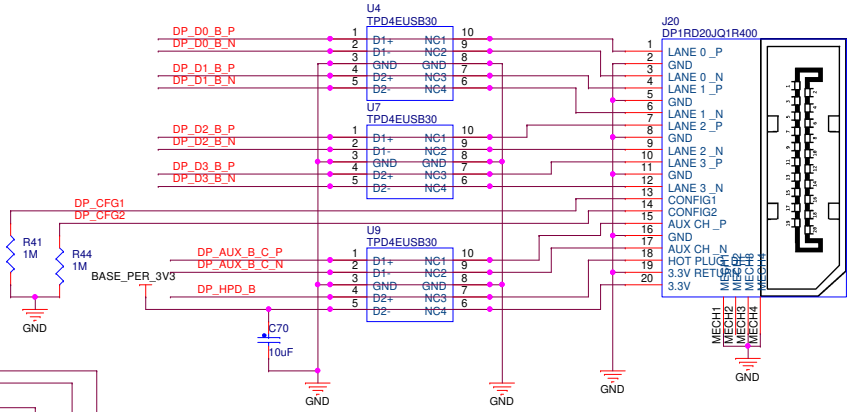
HDMI 2.0a specification (HDMI.org)
DisplayPort 1.3 standard (VESA.org)
Embedded DisplayPort 1.4 standard




## HDMI REFCLK for DART-MX8M Only!

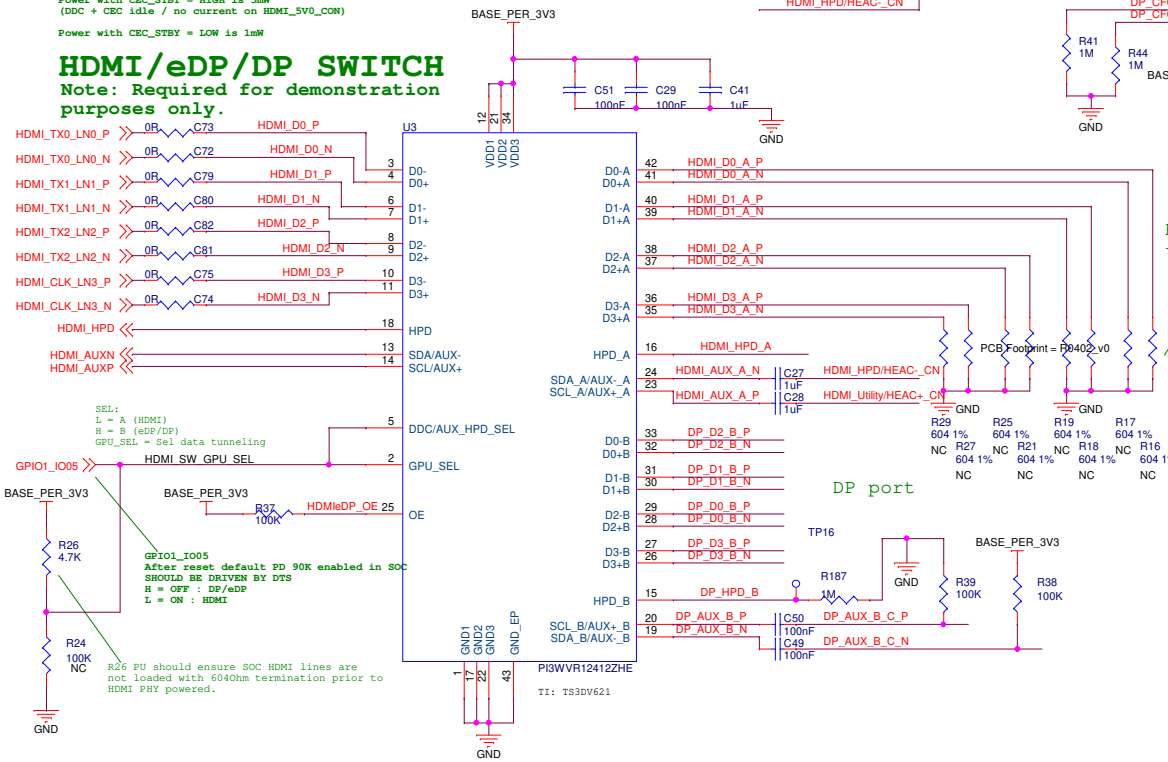



## DP PORT



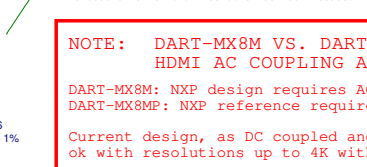

## HDMI/eDP/DP SWITCH

**Note: Required for demonstration purposes only.**




HDMI PORT
+ Level Termination

Note : HDMI pull down must not be applied until VDD_PHY_1V8 is up.
Implemtation uses fact that BASE_PER_3V3 rises after all SOM power rails are up.
At boot time GPIO drives U3 switch to B state.




DP port




NOTE: DART-MX8M VS. DART-MX8M-PLUS
HDMI AC COUPLING AND LEVEL TERMINATION PORT

DART-MX8M: NXP design requires AC coupling and level termination on HDMI path;
DART-MX8MP: NXP reference requires DC coupling with no level termination;

Current design, as DC coupled and no termination, tested ok with resolutions up to 4K with DART-MX8M HDMI and DP path;

Customers designing for DART-MX8M should include C72-C75 C79-C82 as 100nF and R16-R19 R21 R25 R27 R29 as 604 Ohm

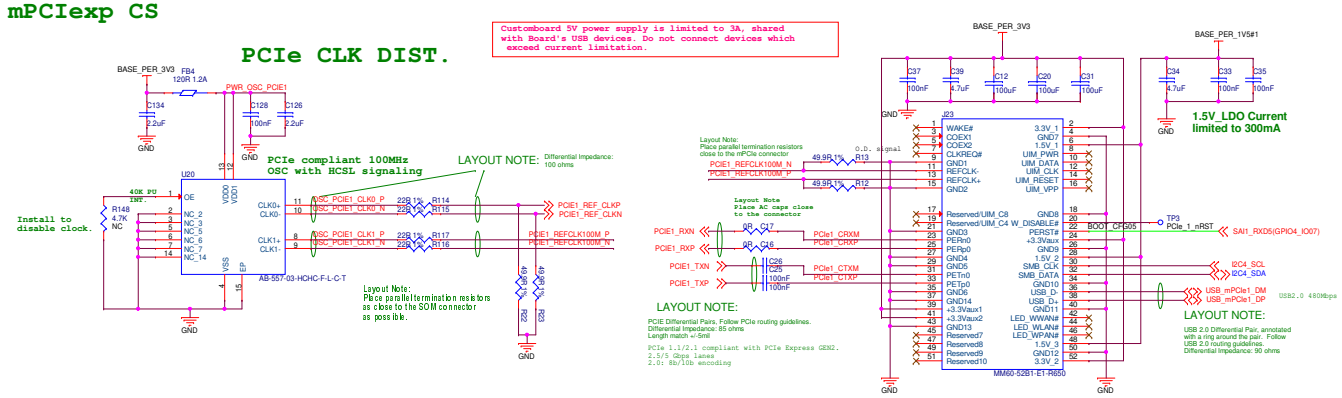
Variscite

| | | | |
|---|---|---|---|
| Title: 06. HDMI , eDP | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: <Approved By> | |
| Date: Wednesday, October 07, 2020 | | Sheet 10 of 17 | |

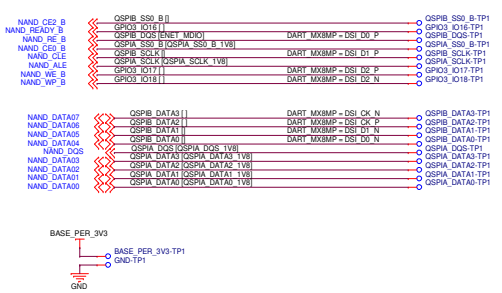
# 07. PCIe, NAND, USB DEBUG

## mPCIexp CS

### PCIe CLK DIST.

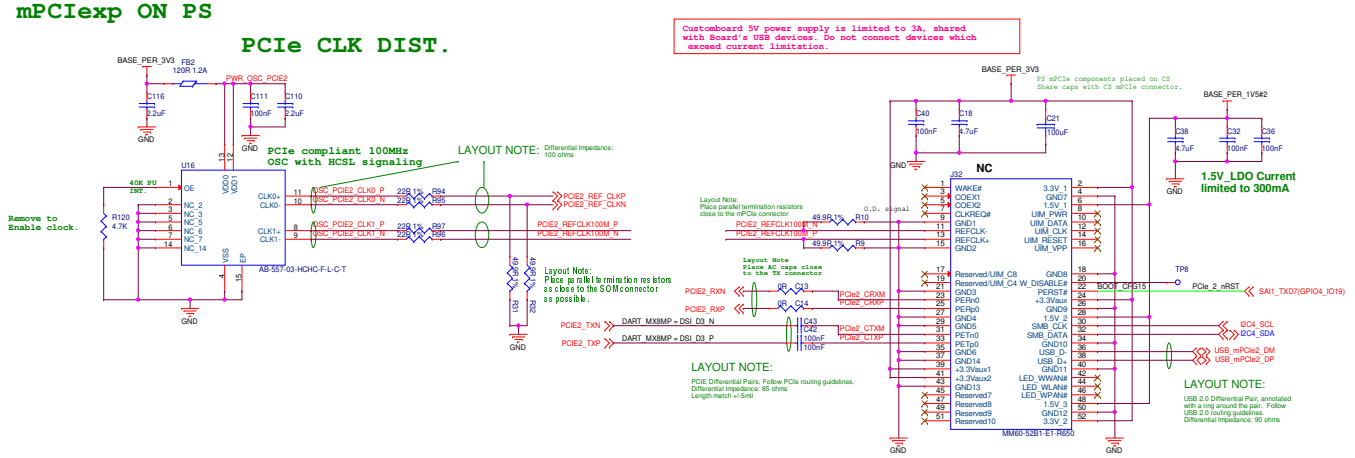



## QSPI TEST POINTS ON PS

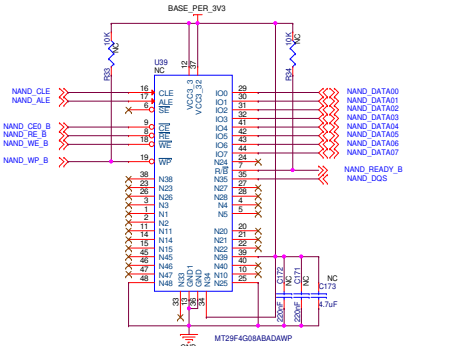


## mPCIexp ON PS

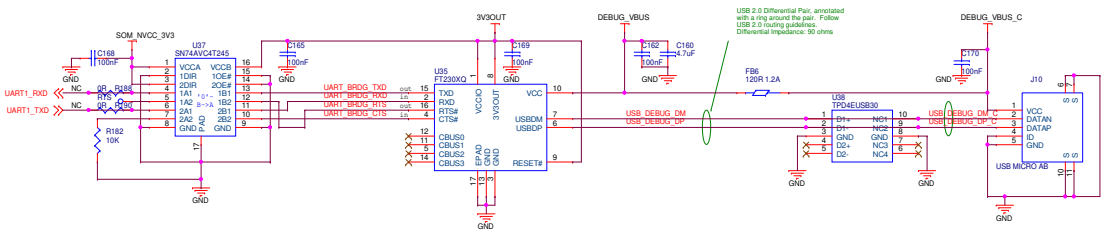
### PCIe CLK DIST.




## NAND



## USB UART DEBUG




Variscite

| | | | |
|---|---|---|---|
| Title: 07. PCIe, NAND, USB DEBUG | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project | Rev: 1.4C-RC1.0 |
| Designer: Oded A. VPC0331 | | Approved By: <Approved By> | |
| Date: Wednesday, October 07, 2020 | | Sheet 11 of 17 | |

# 08. USB TYPE C, USB 3 HUB

## USB#1

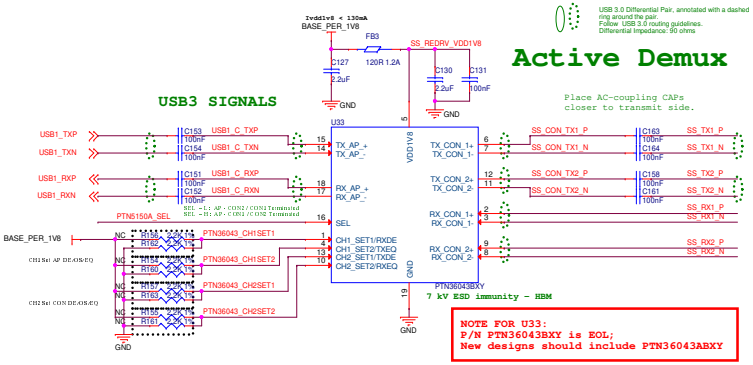
## USB TYPE C OTG

LAYOUT NOTE:
USB 3.0 Differential Pair, annotated with a dashed ring around the pair.
Follow USB 3.0 routing guidelines.
Differential Impedance: 90 ohms

## Active Demux

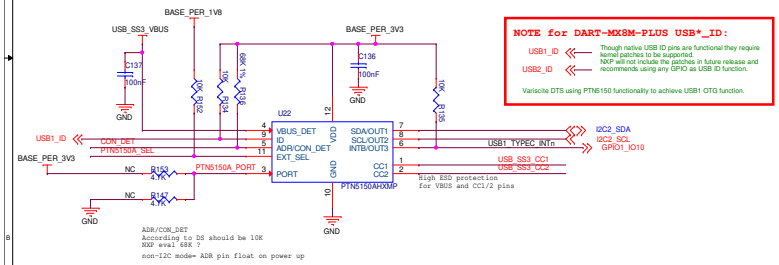
### USB3 SIGNALS

Place AC-coupling CAPs closer to transmit side.




NOTE FOR U33:
P/N PTN36043BXY is EOL;
New designs should include PTN36043ABXY

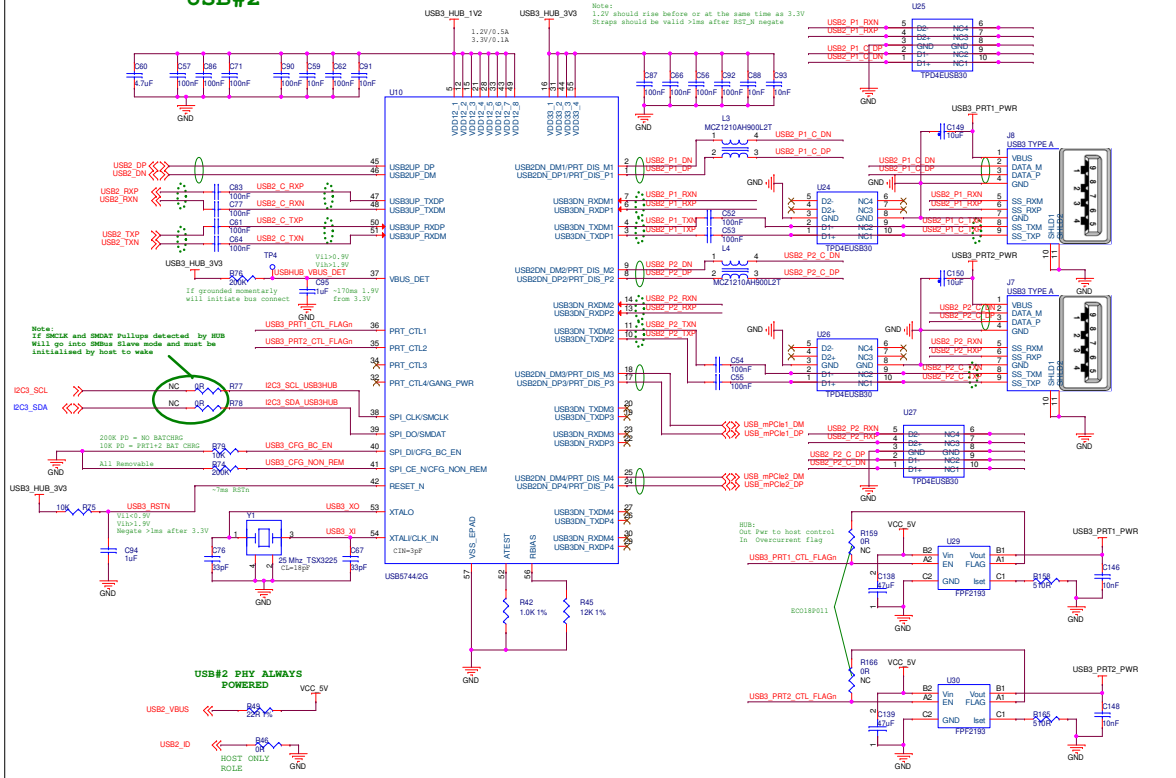
## Config Channel Logic Detection & Indication of Plug Orientation



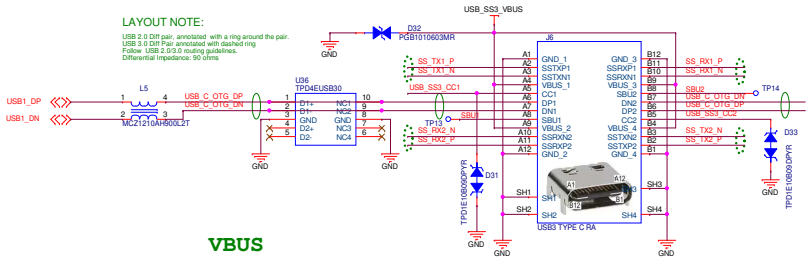

NOTE for DART-MX8M-PLUS USB*_ID:
USB1_ID
USB2_ID
Though native USB ID pins are functional they require kernel patches to be supported.
NXP will not include the patches in future release and recommends using any GPIO as USB ID function.
Variscite DTS using PTN5150 functionality to achieve USB1 OTG function.

## USB3.0 HUB

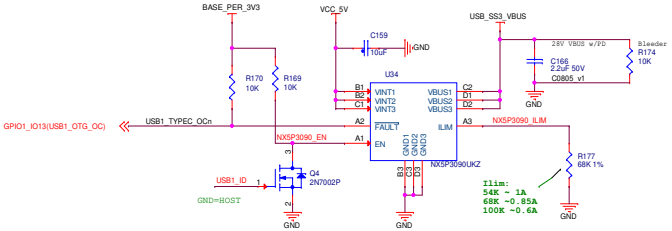
### USB#2




## USB TYPE C OTG



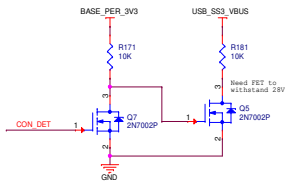

## 5V Source Load Switch

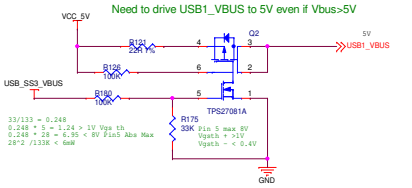


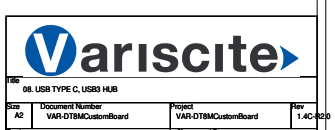

USB Profile 1 = 5 V @ 2 A

1 A current limitation due to system power limitation of CPU Card + Base Board.

## VBUS DISCHARGE

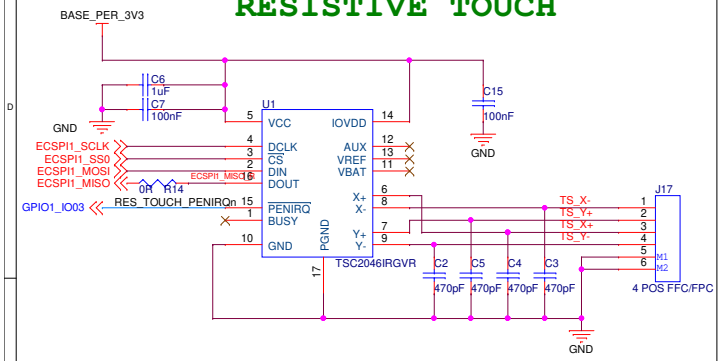


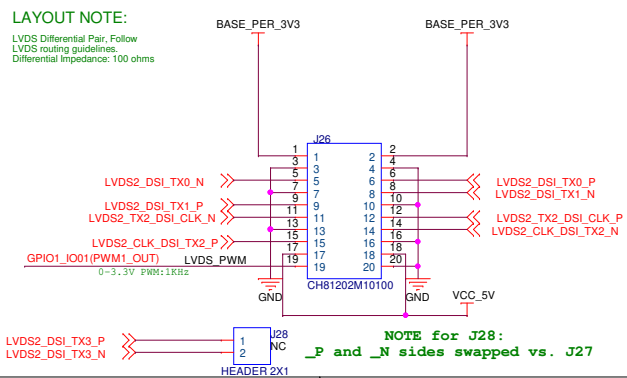



# 09. LVDS, TOUCH, JTAG, GP SW & LEDs

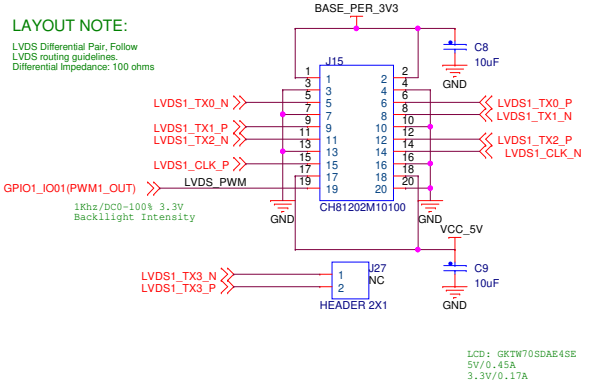
## RESISTIVE TOUCH



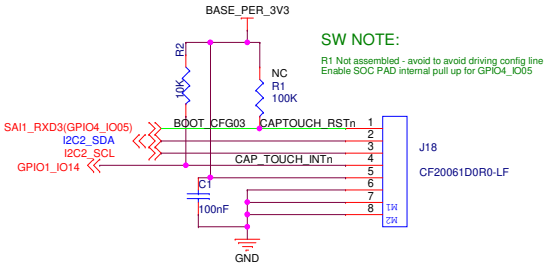

## LVDS CH1 DISPLAY



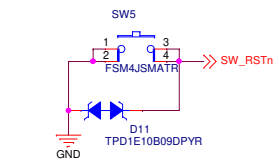

## LVDS DISPLAY CH0




## CAPACITIVE TOUCH



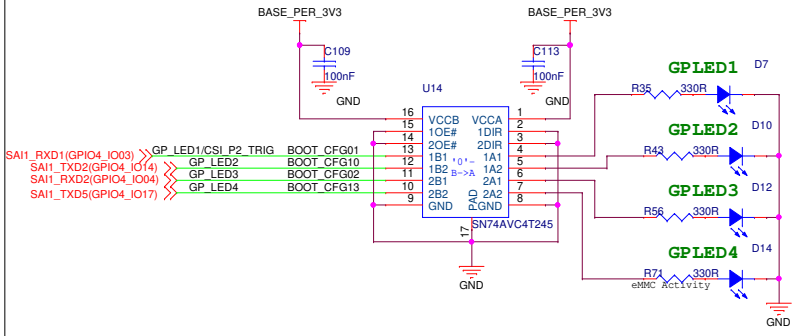

## RST



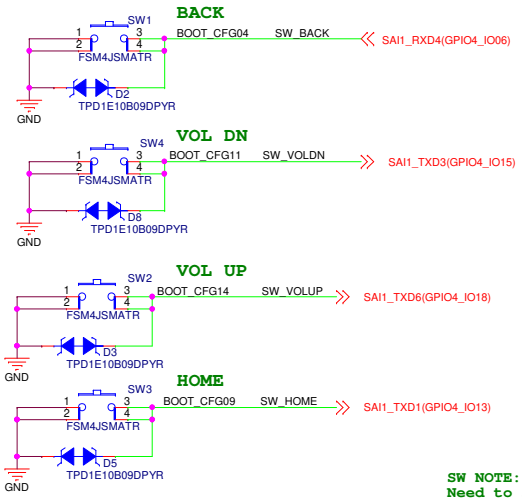

DART-MX8MP-V1.0A Note:

Reset button not usable with DART-MX8MP-Plus-V1.0A as U4 asserts PMIC_ON_REQ which is a push pull on imx8mp SOC vs. open drain on DT8M & DT8M-Mini. PMIC_ON_REQ is replaced with PMIC_RST to acieve correct functionality as off DART-MX8M-Plus-V1.1

## GP LEDS

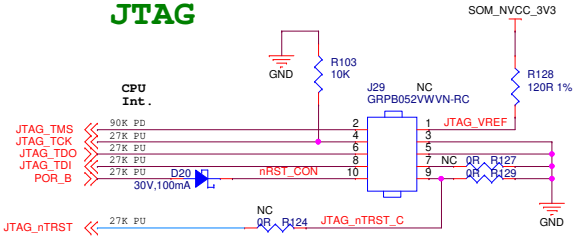



## GP BUTTONS




SW NOTE:
Need to set Int. PU in SOC
on all SWitches

## JTAG




NOTE: DT8MP JTAG_nTRST is JTAG_MODE 10K PD required on SOM

The new 10 pin smaller connector is now becoming an industry standard.

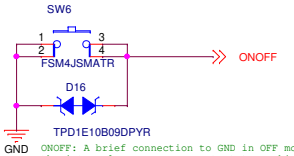
The ARM DStream comes with a 10-pin connector. If you need a ribbon, they can be purhased at Digikey:
Samtec Inc MPN: FFSD-05-D-04.00-01-N

If you need to expand to a 20-pin connector for a different JTAG device, the expander board can also be purchased at Digikey:
Olimex LTD MPN: ARM-JTAG-20-10

https://www.digikey.com/products/en/development-boards-kits-programmers/accessories/783?k=JTAG%20adapter

## ON/OFF

PU Included on SOM



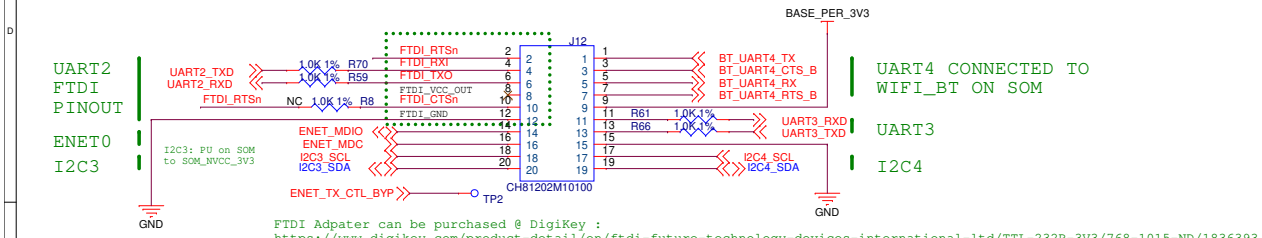

ONOFF: A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). An approximate 5 second or more connection to GND causes a forced OFF.

Not used leave NC

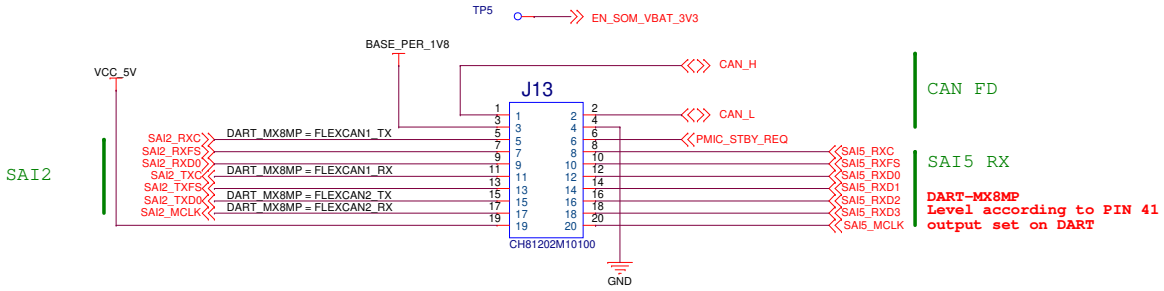
Variscite

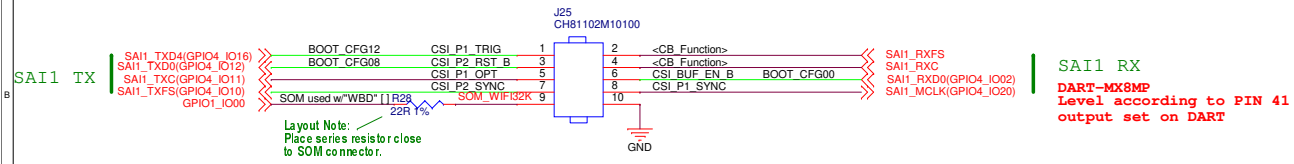
| | | | |
|---|---|---|---|
| Title | 09. LVDS, TOUCH, JTAG, GP SW & LEDs | | |
| Size A3 | Document Number VAR-DT8MCustomBoard | Project VAR-DT8MCustomBoard | Rev 1.4C-R2.0 |
| Designer: | Oded A. VPC0331 | Approved By: | |
| Date: | Wednesday, October 07, 2020 | Sheet 13 of 17 | |

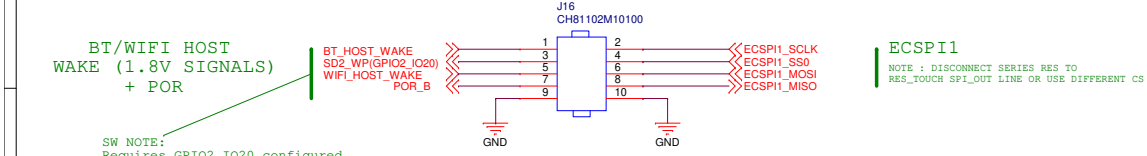
# 10. HEADERS, Pull Ups

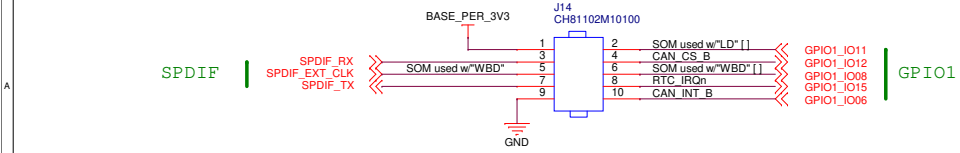


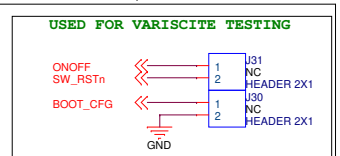

FTDI Adpater can be purchased @ DigiKey :
https://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393
See pinout: http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

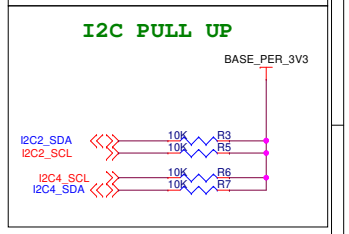


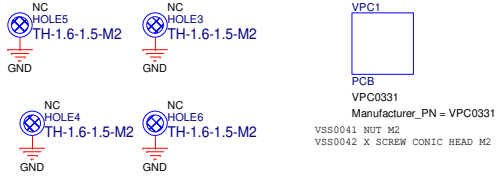



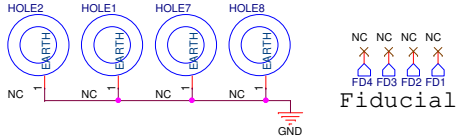




## MECHANICS

SOM MOUNTING STANDOFF
Place on TOP




CHASSIS HOLES




Variscite

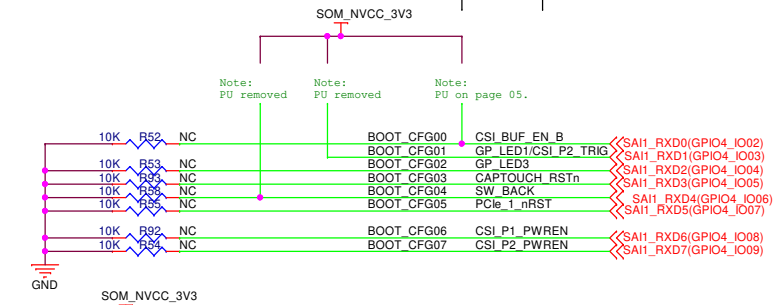
| | | | |
|---|---|---|---|
| Title: 10. HEADERS, Mechanics, Pull Ups | | | |
| Size: A3 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 14 of 17 | |

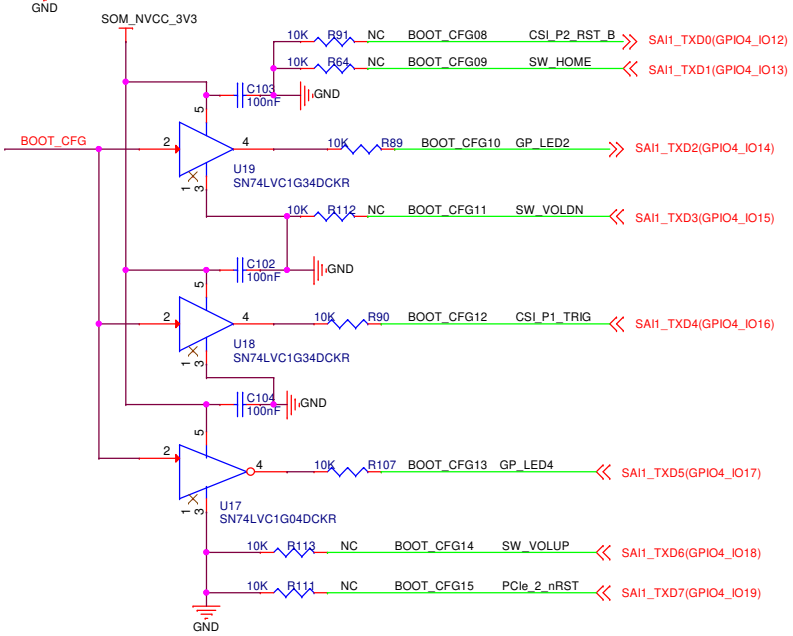
# 11. BOOT CONFIG & MODE

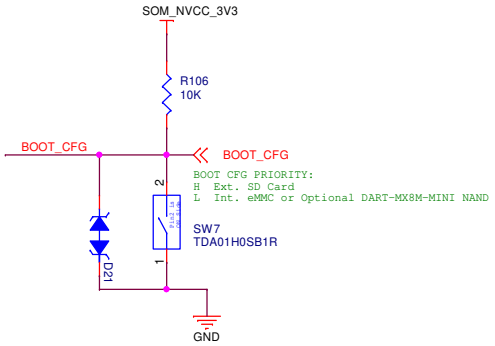
| | | | INT. BOOT | EXT. BOOT | |
|---|---|---|---|---|---|
| SAI1_RXD0(GPIO4_IO02) | CSI_BUF_EN_B | BOOT_CFG00 | 0 | 0 | Need to Enable PU in DTS; See pp. 5 |
| SAI1_RXD1(GPIO4_IO03) | GP_LED1/CSI_P2_TRIG | BOOT_CFG01 | 0 | 0 | |
| SAI1_RXD2(GPIO4_IO04) | GP_LED3 | BOOT_CFG02 | 0 | 0 | |
| SAI1_RXD3(GPIO4_IO05) | CAPTOUCH_RSTn | BOOT_CFG03 | 0 | 0 | |
| SAI1_RXD4(GPIO4_IO06) | SW_BACK | BOOT_CFG04 | 0 | 0 | |
| SAI1_RXD5(GPIO4_IO07) | PCIe_1_nRST | BOOT_CFG05 | 0 | 0 | |
| SAI1_RXD6(GPIO4_IO08) | CSI_P1_PWREN | BOOT_CFG06 | 0 | 0 | |
| SAI1_RXD7(GPIO4_IO09) | CSI_P2_PWREN | BOOT_CFG07 | 0 | 0 | |
| SAI1_TXD0(GPIO4_IO12) | CSI_P2_RST_B | BOOT_CFG08 | 0 | 0 | |
| SAI1_TXD1(GPIO4_IO13) | SW_HOME | BOOT_CFG09 | 0 | 0 | |
| SAI1_TXD2(GPIO4_IO14) | GP_LED2 | BOOT_CFG10 | 0 | 1 | |
| SAI1_TXD3(GPIO4_IO15) | SW_VOLDN | BOOT_CFG11 | 0 | 0 | |
| SAI1_TXD4(GPIO4_IO16) | CSI_P1_TRIG | BOOT_CFG12 | 0 | 1 | |
| SAI1_TXD5(GPIO4_IO17) | GP_LED4 | BOOT_CFG13 | 1 | 0 | |
| SAI1_TXD6(GPIO4_IO18) | SW_VOLUP | BOOT_CFG14 | 0 | 0 | |
| SAI1_TXD7(GPIO4_IO19) | PCIe_2_nRST | BOOT_CFG15 | 0 | 0 | |

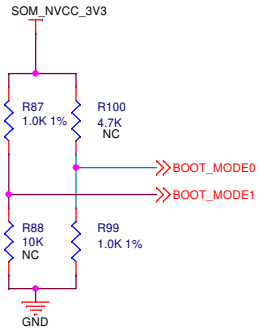
**Notes:**
a. Sampled on rising edge of POR_B
b. 90K ohm Int. SOC PD during POR_B and after on BOOT CFG[15:0] and BOOTMODE[1:0]
c. BOOT_MODE[1:0] ="10" is Internal Boot - Always used.
d. Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

**DART-MX8M-MINI Notes:**
a. Internal boot can be eMMC or NAND(when it is released)
b. Boot config lines do not follow the Mini datasheet in full DART-MX8M-MINI have added logic to be compatible to DART-MX8M
c. Need to modify R90 to 10K (R89 and R107 not a must)




**DART-MX8M-PLUS Notes:**
a. Boot configuration set by BOOT_MODE[0..3]
b. BOOT_MODE0 connected via buffer on DART-MX8MP to SAI1_TXD2

*i.MX8M Plus Boot Mode*

| BOOT_MODE3 | BOOT_MODE2 | BOOT_MODE1 | BOOT_MODE0 | Boot Modes |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Boot From Internal Fuses |
| 0 | 0 | 0 | 1 | USB Serial Download |
| 0 | 0 | 1 | 0 | USDHC3 (eMMC boot only, SD3 8-bit) Default |
| 0 | 0 | 1 | 1 | USDHC2 (SD boot only, SD2) |

| DART-MX8MP Pin: | J1.72 | J2.13 | J2.11 | J2.78 |
|---|---|---|---|---|
| CustomBoard Net: | EN_SOM_VBAT_3V3 | BOOT_MODE0 BOOT_MODE1 | | SAI1_TXD2 |

| | | |
|---|---|---|
| Title: 11. BOOT CONFIG & MODE | | |
| Size: B | Document Number: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Date: Wednesday, October 07, 2020 | Sheet 15 of 17 | |

# 12. PINMUX J1 & J2 & J3

| | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT IC | CB_FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|---|
| NAND_DATA00 | NAND_DATA00 | QSPIA_DATA0 [QSPIA_DATA0_1V8] | | | | GPIO3_IO06 [GPIO3_IO06_1V8] | | | [SOM used w/NAND] | J1 |
| NAND_DATA01 | NAND_DATA01 | QSPIA_DATA1 [QSPIA_DATA1_1V8] | | | | GPIO3_IO07 [GPIO3_IO07_1V8] | | | [SOM used w/NAND] | |
| NAND_DATA02 | NAND_DATA02 | QSPIA_DATA2 [QSPIA_DATA2_1V8] | | | | GPIO3_IO08 [GPIO3_IO08_1V8] | | | [SOM used w/NAND] | |
| NAND_DATA03 | NAND_DATA03 | QSPIA_DATA3 [QSPIA_DATA3_1V8] | | | | GPIO3_IO09 [GPIO3_IO09_1V8] | | | [SOM used w/NAND] | |
| NAND_DATA04 | NAND_DATA04 [NC] | QSPIB_DATA0 [ ] | | | | GPIO3_IO10 [ ] | | | | |
| NAND_DATA05 | NAND_DATA05 [NC] | QSPIB_DATA1 [ ] | | | | GPIO3_IO11 [ ] | | | | |
| NAND_DATA06 | NAND_DATA06 [CLKIN2_1V8] | QSPIB_DATA2 [ ] | | | | GPIO3_IO12 [ ] | | | | |
| NAND_DATA07 | NAND_DATA07 [CLKIN1_1V8] | QSPIB_DATA3 [ ] | | | | GPIO3_IO13 [ ] | | | | |
| NAND_CE0_B | NAND_CE0_B | QSPIA_SS0_B [QSPIA_SS0_B_1V8] | | | | GPIO3_IO01 [GPIO3_IO01_1V8] | | | [SOM used w/NAND] | |
| NAND_CE2_B | NAND_CE2_B [CLKOUT2_1V8] | QSPIB_SS0_B [ ] | | | | GPIO3_IO03 [ ] | | | | |
| NAND_DQS | NAND_DQS | QSPIA_DQS [QSPIA_DQS_1V8] | | | | GPIO3_IO14 [GPIO3_IO14_1V8] | | | [SOM used w/NAND] | |
| NAND_ALE | NAND_ALE | QSPIA_SCLK [QSPIA_SCLK_1V8] | | | | GPIO3_IO00 [GPIO3_IO00_1V8] | | | [SOM used w/NAND] | |
| NAND_WP_B | NAND_WP_B [NC] | | | | | GPIO3_IO18 [ ] | | | | |
| NAND_WE_B | NAND_WE_B [NC] | | | | | GPIO3_IO17 [ ] | | | | |
| NAND_RE_B | NAND_RE_B [GPIO1_IO07] | QSPIB_DQS [ENET_MDIO] | | | | GPIO3_IO15 [ ] | [EXT_CLK4] | | <CB_Function> | |
| NAND_CLE | NAND_CLE [CLKOUT1_1V8] | QSPIB_SCLK [ ] | | | | GPIO3_IO05 [ ] | | | | |
| NAND_READY_B | NAND_READY_B [NC] | | | | | GPIO3_IO16 [ ] | | | | |
| CONN_SD2_CLK | SD2_CLK | | | | | GPIO2_IO13 | | | | |
| CONN_SD2_DATA0 | SD2_DATA0 | | | | | GPIO2_IO15 | | | | |
| CONN_SD2_DATA1 | SD2_DATA1 | | | | | GPIO2_IO16 | | | | |
| CONN_SD2_DATA2 | SD2_DATA2 | | | | | GPIO2_IO17 | | | | |
| CONN_SD2_DATA3 | SD2_DATA3 | | | | | GPIO2_IO18 | | | | |
| CONN_SD2_CMD | SD2_CMD | | | | | GPIO2_IO14 | | | | |
| CONN_SD2_CD_B | SD2_CD_B | | | | | GPIO2_IO12 | | | | |
| CONN_SD2_nRST | SD2_RESET_B | | | | | GPIO2_IO19 | | | SD2_PWR_CTRL | |
| SD2_WP(GPIO2_IO20) | SD2_WP [SD1_DATA7] | | | | | GPIO2_IO20 [GPIO2_IO09_1V8] | | | | |
| ETH_TRX0_N | ENET_TD2 | ENET_TX_CLK_IN/ENET_REF_CLK_ROOT_OUT | | | | GPIO1_IO19 | | ETH_TRX0_N | | |
| ETH_TRX0_P | ENET_TD3 | | | | | GPIO1_IO18 | | ETH_TRX0_P | | |
| ETH_TRX1_N | ENET_TD0 | | | | | GPIO1_IO21 | | ETH_TRX1_N | | |
| ETH_TRX1_P | ENET_TD1 | | | | | GPIO1_IO20 | | ETH_TRX1_P | | |
| ETH_TRX2_N | ENET_RD1 | | | | | GPIO1_IO27 | | ETH_TRX2_N | | |
| ETH_TRX2_P | ENET_RD0 | | | | | GPIO1_IO26 | | ETH_TRX2_P | | |
| ETH_TRX3_N | ENET_RD3 | | | | | GPIO1_IO29 | | ETH_TRX3_N | | |
| ETH_TRX3_P | ENET_RD2 | | | | | GPIO1_IO28 | | ETH_TRX3_P | | |
| ENET_TX_CTL_8YP | ENET_TX_CTL | | | | | GPIO1_IO22 | | NC | | |
| LED_LINK10_100 | ENET_TXC | ENET_TX_ER | | | | GPIO1_IO23 | | LED_LINK10_100 | | |
| LED_LINK1000 | ENET_RXC | ENET_RX_ER | | | | GPIO1_IO25 | | LED_LINK1000 | | |
| LED_ACT | ENET_RX_CTL | | | | | GPIO1_IO24 | | LED_ACT | | |
| ENET_MDIO | ENET_MDIO | | | | | GPIO1_IO17 | | | SOM used w/"EC" | |
| ENET_MDC | ENET_MDC | | | | | GPIO1_IO16 | | | SOM used w/"EC" | |
| GPIO1_IO00 | GPIO1_IO00 | ENET_PHY_REF_CLK_ROOT_OUT | | | | REF_CLK_32K | EXT_CLK1 | | SOM used w/"WBD" [ ] | |
| I2C4_SCL | I2C4_SCL | PWM2_OUT | PCIE1_CLKREQ_B | | | GPIO5_IO20 | | | | |
| I2C4_SDA | I2C4_SDA | PWM1_OUT | PCIE2_CLKREQ_B [ ] | | | GPIO5_IO21 | | | | |
| HPLOUT | SAI3_RXD | GPT1_COMPARE1 | SAI5_RXD0 | | | GPIO4_IO30 | | HPLOUT | | J2 |
| HPROUT | SAI3_TXC | GPT1_COMPARE2 | SAI5_RXD2 | | [UART2_TXD] | GPIO5_IO00 | | HPROUT | | |
| HPOUTFB | SAI3_RXFS | GPT1_CAPTURE1 | SAI5_RXFS | [SAI3_RXD1] | | GPIO4_IO28 | | HPOUTFB | | |
| LINEIN1_LP | SAI3_RXC | GPT1_CAPTURE2 [GPT1_CLK] | SAI5_RXC | | [UART2_CTS_B] | GPIO4_IO29 | | LINEIN1_LP | | |
| LINEIN1_RP | SAI3_TXFS | GPT1_CLK [GPT1_CAPTURE2] | SAI5_RXD1 | [SAI3_TXD1] | [UART2_RXD] | GPIO4_IO31 | | LINEIN1_RP | | |
| DMIC_CLK | SAI3_TXD | GPT1_COMPARE3 | SAI5_RXD3 | | | GPIO5_IO01 | | DMIC_CLK | | |
| DMIC_DATA | SAI3_MCLK | PWM4_OUT | SAI5_MCLK | | | GPIO5_IO02 | | DMIC_DATA | | |
| BT_UART4_TX | ECSPI2_MOSI | UART4_TXD | | | | GPIO5_IO11 | | | SOM used w/"WBD" | |
| BT_UART4_CTS_B | ECSPI2_MISO | UART4_CTS_B | | | | GPIO5_IO12 | | | SOM used w/"WBD" | |
| BT_UART4_RX | ECSPI2_SCLK | UART4_RXD | | | | GPIO5_IO10 | | | SOM used w/"WBD" | |
| BT_UART4_RTS_B | ECSPI2_SS0 | UART4_RTS_B | | | | GPIO5_IO13 | | | SOM used w/"WBD" | |
| GPIO1_IO02(nWDOG) | GPIO1_IO02 | WDOG_B | | | | [WDOG_ANY] | | | WDOGin | |
| I2C2_SDA | I2C2_SDA | ENET1_1588_EVENT1_OUT | | | | GPIO5_IO17 | | | | |
| I2C2_SCL | I2C2_SCL | ENET1_1588_EVENT1_IN | | | | GPIO5_IO16 | | | | |
| ECSPI1_SCLK | ECSPI1_SCLK | UART3_RXD | | | | GPIO5_IO06 | | | | |
| ECSPI1_SS0 | ECSPI1_SS0 | UART3_RTS_B | | | | GPIO5_IO09 | | | | |
| ECSPI1_MISO | ECSPI1_MISO | UART3_CTS_B | | | | GPIO5_IO08 | | | | |
| ECSPI1_MOSI | ECSPI1_MOSI | UART3_TXD | | | | GPIO5_IO07 | | | | |
| UART1_RXD | UART1_RXD | ECSPI3_SCLK | | | | GPIO5_IO22 | | | | |
| UART1_TXD | UART1_TXD | ECSPI3_MOSI | | | | GPIO5_IO23 | | | | |
| UART2_RXD | UART2_RXD | ECSPI3_MISO | | | | GPIO5_IO24 | | | | |
| UART2_TXD | UART2_TXD | ECSPI3_SS0 | | | | GPIO5_IO25 | | | | |
| UART3_RXD | UART3_RXD | UART1_CTS_B | | | | GPIO5_IO26 | | | | |
| UART3_TXD | UART3_TXD | UART1_RTS_B | | | | GPIO5_IO27 | | | | |
| SAI2_MCLK | SAI2_MCLK | SAI5_MCLK | | | | GPIO4_IO27 | | | | |
| SAI2_RXFS | SAI2_RXFS | SAI5_TXFS | [SAI5_TXD1] | [SAI2_RXD1] | [UART1_TXD] | GPIO4_IO21 | | | | |
| SAI2_RXC | SAI2_RXC | SAI5_TXC | | | [UART1_RXD] | GPIO4_IO22 | | | | |
| SAI2_TXFS | SAI2_TXFS | SAI5_TXD1 | | [SAI2_TXD1] | [UART1_CTS_B] | GPIO4_IO24 | | | | |
| SAI2_TXC | SAI2_TXC | SAI5_TXD2 | | | | GPIO4_IO25 | | | | |
| SAI2_RXD0 | SAI2_RXD0 | SAI5_TXD0 | | | [UART1_RTS_B] | GPIO4_IO23 | | | | |
| SAI2_TXD0 | SAI2_TXD0 | SAI5_TXD3 | | | | GPIO4_IO26 | | | | |
| SAI5_MCLK | SAI5_MCLK | SAI1_TXC | SAI4_MCLK [ ] | | | GPIO3_IO25 | | | | |
| SAI5_RXFS | SAI5_RXFS | SAI1_TXD0 | | | | GPIO3_IO19 | | | | |
| SAI5_RXC | SAI5_RXC | SAI1_TXD1 | | | [PDM_CLK] | GPIO3_IO20 | | | | |
| SAI5_RXD0 | SAI5_RXD0 | SAI1_TXD2 | | | [PDM_BIT0] | GPIO3_IO21 | | | | |
| SAI5_RXD1 | SAI5_RXD1 | SAI1_TXD3 | SAI1_TXFS | SAI5_TXFS | [PDM_BIT1] | GPIO3_IO22 | | | | |
| SAI5_RXD2 | SAI5_RXD2 | SAI1_TXD4 | SAI1_TXFS | SAI5_TXC | [PDM_BIT2] | GPIO3_IO23 | | | | |
| SAI5_RXD3 | SAI5_RXD3 | SAI1_TXD5 | SAI1_TXFS | SAI5_TXD0 | [PDM_BIT3] | GPIO3_IO24 | | | | |
| SAI1_MCLK(GPIO4_IO20) | SAI1_MCLK | SAI5_MCLK | SAI1_TXC | [PDM_CLK] | | GPIO4_IO20 | | | CSI_P1_SYNC | |
| SAI1_RXFS | SAI1_RXFS | SAI5_RXFS | | | | GPIO4_IO00 | | | | |
| SAI1_RXC | SAI1_RXC | SAI5_RXC | | | | GPIO4_IO01 | | | | |
| SAI1_TXFS(GPIO4_IO10) | SAI1_TXFS | SAI5_TXFS | | | | GPIO4_IO10 | | | CSI_P2_SYNC | |
| SAI1_TXC(GPIO4_IO11) | SAI1_TXC | SAI5_RXD0 | | | | GPIO4_IO11 | | | CSI_P1_OPT | |
| SAI1_RXD0(GPIO4_IO02) | SAI1_RXD0 | SAI6_RXD0 | [SAI1_TXD1] | [PDM_BIT0] | | GPIO4_IO02 | BOOT_CFG00 | | CSI_BUF_EN_B | |
| SAI1_RXD1(GPIO4_IO03) | SAI1_RXD1 | SAI6_RXD1 | | [PDM_BIT1] | | GPIO4_IO03 | BOOT_CFG01 | | GP_LED1/CSI_P2_TRIG | |
| SAI1_RXD2(GPIO4_IO04) | SAI1_RXD2 | SAI6_RXD2 | | [PDM_BIT2] | | GPIO4_IO04 | BOOT_CFG02 | | GP_LED3 | |
| SAI1_RXD3(GPIO4_IO05) | SAI1_RXD3 | SAI6_RXD3 | | [PDM_BIT3] | | GPIO4_IO05 | BOOT_CFG03 | | CAPTOUCH_RSTn | |
| SAI1_RXD4(GPIO4_IO05) | SAI1_RXD4 | SAI6_TXC | SAI6_RXC | | | GPIO4_IO06 | BOOT_CFG04 | | SW_BACK | |
| SAI1_RXD5(GPIO4_IO07) | SAI1_RXD5 | SAI6_TXD0 | SAI6_RXD0 | SAI1_RXFS | | GPIO4_IO07 | BOOT_CFG05 | | PCIe_1_nRST | |
| SAI1_RXD6(GPIO4_IO08) | SAI1_RXD6 | SAI6_TX_SYNC | SAI6_RXFS | | | GPIO4_IO08 | BOOT_CFG06 | | CSI_P1_PWREN | |
| SAI1_RXD7(GPIO4_IO09) | SAI1_RXD7 | SAI6_MCLK | SAI1_TXFS | SAI1_TXD4 | | GPIO4_IO09 | BOOT_CFG07 | | CSI_P2_PWREN | |
| SAI1_TXD0(GPIO4_IO12) | SAI1_TXD0 | SAI5_TXD0 | | | | GPIO4_IO12 | BOOT_CFG08 | | CSI_P2_RST_B | |
| SAI1_TXD1(GPIO4_IO13) | SAI1_TXD1 | SAI5_TXD1 | | | | GPIO4_IO13 | BOOT_CFG09 | | SW_HOME | |
| SAI1_TXD2(GPIO4_IO14) | SAI1_TXD2 | SAI5_TXD2 | | | | GPIO4_IO14 | BOOT_CFG10 | | GP_LED2 | |
| SAI1_TXD3(GPIO4_IO15) | SAI1_TXD3 | SAI5_TXD3 | | | | GPIO4_IO15 | BOOT_CFG11 | | SW_VOLDN | |
| SAI1_TXD4(GPIO4_IO16) | SAI1_TXD4 | SAI6_RXC | SAI6_TXC | | | GPIO4_IO16 | BOOT_CFG12 | | CSI_P1_TRIG | |
| SAI1_TXD5(GPIO4_IO17) | SAI1_TXD5 | SAI6_RXD0 | SAI6_TXD0 | | | GPIO4_IO17 | BOOT_CFG13 | | GP_LED4 | |
| SAI1_TXD6(GPIO4_IO18) | SAI1_TXD6 | SAI6_RXFS | SAI6_TXFS | | | GPIO4_IO18 | BOOT_CFG14 | | SW_VOLUP | |
| SAI1_TXD7(GPIO4_IO19) | SAI1_TXD7 | SAI6_MCLK | | [PDM_CLK] | | GPIO4_IO19 | BOOT_CFG15 | | PCIe_2_nRST | |
| UART4_TXD(GPIO5_IO29) | UART4_TXD | UART2_RTS_B | PCIE2_CLKREQ_B [ ] | | | GPIO5_IO29 | | | CSI_P2_OPT | J3 |
| UART4_RXD(GPIO5_IO28) | UART4_RXD | UART2_CTS_B | PCIE1_CLKREQ_B | | | GPIO5_IO28 | | | CSI_P1_RST_B | |
| SPDIF_RX | SPDIF_RX | PWM2_OUT | | | | GPIO5_IO04 | | | | |
| SPDIF_TX | SPDIF_TX | PWM3_OUT | | | | GPIO5_IO03 | | | | |
| SPDIF_EXT_CLK | SPDIF_EXT_CLK | PWM1_OUT | | | | GPIO5_IO05 | | | SOM used w/"WBD" | |
| I2C3_SDA | I2C3_SDA | PWM3_OUT | GPT3_CLK | | | GPIO5_IO19 | | | SOM Shared | |
| I2C3_SCL | I2C3_SCL | PWM4_OUT | GPT2_CLK | | | GPIO5_IO18 | | | SOM Shared | |
| GPIO1_IO01(PWM1_OUT) | GPIO1_IO01 | PWM1_OUT | | | | REF_CLK_24M | EXT_CLK2 | | LVDS_PWM | |
| GPIO1_IO03 | GPIO1_IO03 | USDHC1_VSELECT | | | | | XTAL_OK [ ] | | RES_TOUCH_PENIRQn | |
| GPIO1_IO05 | GPIO1_IO05 | M4_NMI | | | | PMIC_READY | | | HDMI_SW_GPU_SEL | |
| GPIO1_IO06 | GPIO1_IO06 | ENET1_MDC | | | | SD1_CD_B | EXT_CLK3 | | CAN_INT_B | |
| GPIO1_IO08 | GPIO1_IO08 | ENET1_1588_EVENT0_IN | | | | SD2_RESET_B | | | SOM used w/"WBD" [ ] | |
| GPIO1_IO10 | GPIO1_IO10 | USB1_OTG_ID | | | | | | | USB1_TYPEC_INTn | |
| GPIO1_IO11 | GPIO1_IO11 | USB2_OTG_ID | | | | PMIC_READY [ ] | | | SOM used w/"LD" [ ] | |
| GPIO1_IO12 | GPIO1_IO12 | USB1_OTG_PWR | | | | | | | CAN_CS_B | |
| GPIO1_IO13(USB1_OTG_OC) | GPIO1_IO13 | USB1_OTG_OC | | | | PWM2_OUT | | | USB1_TYPEC_OCn | |
| GPIO1_IO14 | GPIO1_IO14 | USB2_OTG_PWR | | | | PWM3_OUT | [CLKO1] | | CAP_TOUCH_INTn | |
| GPIO1_IO15 | GPIO1_IO15 | USB2_OTG_OC | | | | PWM4_OUT | CLKO2 [CLKO1] | | RTC_IRQn | |
| LVDS2_CLK_DSI_TX2_P | DSI_TX2_P | | | | | | | LVDS2_CLK_P | | |
| LVDS2_CLK_DSI_TX2_N | DSI_TX2_N | | | | | | | LVDS2_CLK_N | | |
| LVDS2_DSI_TX0_P | DSI_TX0_P | | | | | | | LVDS2_TX0_P | | |
| LVDS2_DSI_TX0_N | DSI_TX0_N | | | | | | | LVDS2_TX0_N | | |
| LVDS2_DSI_TX1_P | DSI_TX1_P | | | | | | | LVDS2_TX1_P | | |
| LVDS2_DSI_TX1_N | DSI_TX1_N | | | | | | | LVDS2_TX1_N | | |
| LVDS2_TX2_DSI_CLK_P | DSI_CLK_P | | | | | | | LVDS2_TX2_P | | |
| LVDS2_TX2_DSI_CLK_N | DSI_CLK_N | | | | | | | LVDS2_TX2_N | | |
| LVDS2_DSI_TX3_P | DSI_TX3_P | | | | | | | LVDS2_TX3_P | | |
| LVDS2_DSI_TX3_N | DSI_TX3_N | | | | | | | LVDS2_TX3_N | | |
| LVDS1_CLK_P | NC | | | | | | | LVDS1_CLK_P | | |
| LVDS1_CLK_N | NC | | | | | | | LVDS1_CLK_N | | |
| LVDS1_TX0_P | NC | | | | | | | LVDS1_TX0_P | | |
| LVDS1_TX0_N | NC | | | | | | | LVDS1_TX0_N | | |
| LVDS1_TX1_P | NC | | | | | | | LVDS1_TX1_P | | |
| LVDS1_TX1_N | NC | | | | | | | LVDS1_TX1_N | | |
| LVDS1_TX2_P | NC | | | | | | | LVDS1_TX2_P | | |
| LVDS1_TX2_N | NC | | | | | | | LVDS1_TX2_N | | |
| LVDS1_TX3_P | NC | | | | | | | LVDS1_TX3_P | | |
| LVDS1_TX3_N | NC | | | | | | | LVDS1_TX3_N | | |

NOTE:

1. NOTE CB_FUNCTION FOR "SOM used", WHICH MEANS SIGNAL USED ON SOME SOMs WITH OPTIONAL OREDERABLE CONFIGURATIONS. PLEASE REFER TO SOM DATASHEET FOR FURTHER DETAILS.
2. ALT0 TO ALT6 DENOTE ALTERNATE FUNCTIONS OF SOC PINS WHEN USED.
3. ALT IC DENOTE AN ALTERNATE FUNCTION WHEN RELEVANT SOM ORDERABLE CONFIGURATION CHOOSEN. FUNCTION GENERATED BY ALTERNATIVE IC WHEN USED. WHEN DESIGN WITH ALT IC - ALT0 TO ALT6 CANNOT BE USED!
4. GREEN NETS DENOTE PINS USED FOR BOOT CONFIGURATION DURING POWER UP. CARE SHOULD BE GIVEN NOT TO DRIVE THESE LINES BEFORE RISE OF POR_B+1ms.

DART-MX8M-Mini differences:

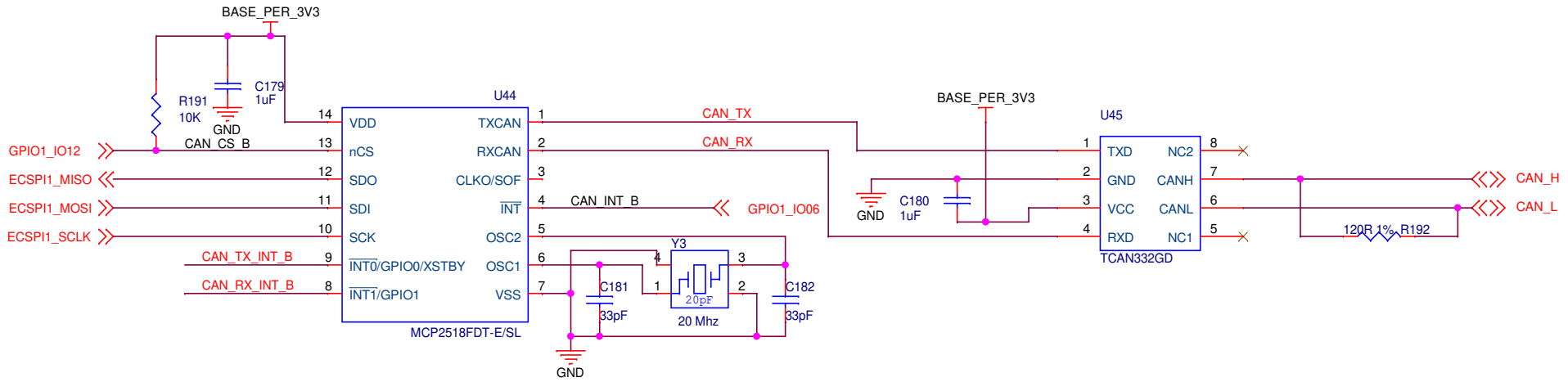
[ ] square brackets are related alternate function to MINI only.
Empty brackets means function removed.

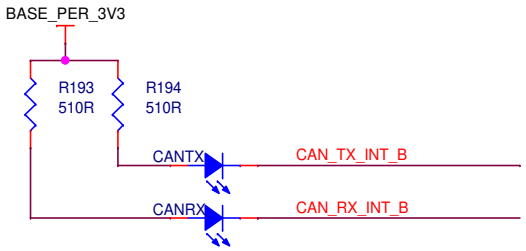
1. PMIC_ON_REQ + PMIC_STBY_REQ + POR_B + ONOFF run @ 1.8V
2. PCIe port 2 does not exist
3. MIPI-CSI port 2 does not exist
4. USB3.0 does not exist on port 1 and 2
5. HDMI does not exist
6. QSPIB does not exist
7. QSPIA exist only with eMMC on SOM and run @ 1.8V

Variscite

| | | | |
|---|---|---|---|
| Title: 12. PINMUX J1 & J2 & J3 | | | |
| Size: A2 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC/0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 16 of 17 | |

# 13. CAN FD Interface




**Note for U44:**
**Recommneded PN for new design MCP2518FDT-E/SL**
**Assembled board can have MCP2517FDT-H/SL**

Variscite

| | | | |
|---|---|---|---|
| Title: CAN FD Interface | | | |
| Size: A4 | Document Number: VAR-DT8MCustomBoard | Project: VAR-DT8MCustomBoard | Rev: 1.4C-R2.0 |
| Designer: Oded A. VPC0331 | | Approved By: | |
| Date: Wednesday, October 07, 2020 | | Sheet 17 of 17 | |