Revision History

Document: Symphony-Board

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Disclaimer:

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Project: Symphony-Board

Date: 24 Monday, April 04, 2022

Approved By: Aviad H.
08. Ethernet

Header/Stub isolation resistors

- J14.1-ENET1_RGMII_TXD0
- J14.1-ENET1_RGMII_TXD1
- J14.1-ENET1_RGMII_TXD2
- J14.1-ENET1_RGMII_TXD3
- J14.2-ENET1_RGMII_RXD0
- J14.2-ENET1_RGMII_RXD1
- J14.2-ENET1_RGMII_RXD2
- J14.2-ENET1_RGMII_RXD3

Note:
Customer requiring usage of J30 header (located on bottom side) should assemble these resistors if not assembled by default.

VDD_ENET for SOM-MX8/MX8X/MX8MP

Power for ENET1: RGMII IDs on SOM power fed from pin J1.38 for specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY

Gigabit Ethernet (Internal)

LAYOUT NOTE:
Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines. Differential Impedance: 100 Ohms

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Note: 1. Default always ON, To disable clock install R21.
2. Replacement PN: AB-557-03-HCHC-F-L.
3. Disabled with SW6 in ON state.

Differential Impedance: 100 ohms

LAYOUT NOTE:
PCIE Differential Pairs, Follow PCIe routing guidelines. Differential Impedance: 85 ohms
Length match +/-5mil

1.5V_LDO Current limited to 300mA

PCIe_CLK

R22, R23, R35, R36 assembled with Ferrite Bead P/N: BLM15BA330SN1D for EMI suppression

FOR SOM-MX6 using internal SoC clock: install 100nF instead of R37, R38
remove R22, R23, R35, R36

Place parallel termination resistors close to the SOM connector as possible.

Place parallel termination resistors close to the mPCIe connector

Place AC caps close to the connector

PCIE Differential Pairs, Follow PCIe routing guidelines. Differential Impedance: 85 ohms
Length match +/-5mil
10. Debug, GPIO Exp, Buttons, LED

**USB UART DEBUG**

- **USB 2.0 Differential Pair,** annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
- **Length Match:** +/- 100 mils
- **Differential Impedance:** 90 ohms

**LAYOUT NOTE:**
- USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines. Length Match: +/- 100 mils. Differential Impedance: 90 ohms

**GPIO EXPANDER**

In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V.
- When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

**GP BUTTON**

- **SW1**
  - **BACK**
  - **EXP_SW1**
- **SW2**
  - **HOLD**
  - **EXP_SW2**
- **SW3**
  - **EXP_SW3**

**GP LED**

- **SW1**
  - **BACK**
  - **EXP_SW1**
- **SW2**
  - **HOLD**
  - **EXP_SW2**
- **SW3**
  - **EXP_SW3**

**Variscite**

- **USB DEBUG DM**
- **USB DEBUG DP**
- **DEBUG_VBUS**
- **BASE_PER_3V3**
- **3V3OUT**
- **GND**
- **USB_DM**
- **USB_DP**
- **DEBUG_VBUS_C**
11. LVDS, DSI, Touch

**LVDS DISPLAY A**

**LVDS DISPLAY B**

**RESISTIVE TOUCH**

**CAPACITIVE TOUCH**

**MIPI DSI DISPLAY**

![Diagram of LVDS, DSI, Touch connections]

**Layout Note:** LVDS Differential Pairs, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

**Note:** It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression.

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See note in: "Headers" Page 14
12. USB2 Host

USB2 Host

LAYOUT NOTE:
- USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
- Length Match: +/- 100 mils
- Differential Impedance: 90 ohms

NOTE:
- Power always enabled; in order to control the power see page 14 "Headers"
13. USB3, uSATA

SATA/USB select

USB TYPE C Circuitry

5V Source Load Switch

SATA 2.0

Config Channel Logic Detection & Indication of Plug Orientation

Usage of native USB_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.

For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI

USB#B_OTG_ID can be left floating if not used.

5V Source Load Switch
14. Headers

Headers arranged for compatible alternate function

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<td>PWMB CPT_INT</td>
<td>UART1 TX</td>
<td>UART1 RX</td>
<td>UART2 TX</td>
<td>UART2 RX</td>
<td>UART1 CTS_B</td>
<td>UARNTX RX</td>
<td>UART1 RTS_B</td>
<td>PWMC</td>
<td>UARTMB TX</td>
<td>UARTMB RX</td>
</tr>
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</table>

| PWM#B | UART#A | UART#B | PWMC | BT_UART |

I2C PULL UPS

- I2C_A has internal pulls in Camera buffer
- I2C_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs
- For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Located on PS

- UART/QSPI
- SAI/SPI
- PWM#B
- UART#A
- UART#B
- PWMC
- BT_UART

Headers arranged for partial compatible alternate function

<table>
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<tr>
<th>J16</th>
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<td>SAIA_RXFS_PCIEA_RESET_B</td>
<td>SIAA_TX</td>
<td>SIAA_RX</td>
<td>SIAA_TXD</td>
<td>SIAA_TXE</td>
<td>DCA_B_SCL</td>
<td>DCA_B_SDA</td>
<td>CAN</td>
<td>SAI</td>
<td>I2C_A</td>
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<td>J1.86-MPI_CAM_BUF_CTL</td>
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<td>J1.82</td>
<td>J1.81-USB3_INTB</td>
<td>J1.80-MIPI_CAM_OPT</td>
<td>J1.79-MIPI_CAM_RST</td>
<td>J1.78-MIPI_CAM_SYNC</td>
<td>J1.77-MIPI_CAM_TRIGGER</td>
<td>J1.76-MIPI_CAM_RST</td>
<td>J1.75-MIPI_CAM_RST</td>
<td>J1.74-MPI_CAM_RST</td>
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COLD RESET ON WDOG_B EVENT for MX6/SOLO and 6UL SOMs

- Listed above SOMs require short on headers to get "Reboot" to function.
- For all other watch dog looped on SOM COLD RESET ON WDOG_B EVENT

USB#A Host VBUS power control

- In order to control the USB#A HOST VBUS power a short is required:
  - Symphony Board reset: See J3.17
  - Symphony Board WDOG_B: See J3.11
  - Symphony Board USB2: See J3.12
  - Symphony Board USB3: See J3.18
  - Symphony Board USB4: See J3.18

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS " located at:
PIN NAMING INSTRUCTIONS:

"/" = Prefix number of "/' denotes alternate function number; none is ALTSAD name

"/" = Prefix denotes pin connected to a configurable module on SOM.
E.g. with "EC" pin EMST_TD0///G52010D78///ETH_TX0_P source is Ethernet PHY

"/" = Prefix points to an alternate function optionally used or shared on SOM;
Verify with SOM datasheet before using this pin;