VAR-SP8CustomBoard

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Disclaimer:

Schematics are for reference only. Variscite LTD provides no warranty for the use of these schematics. Schematics are subject to change without notice.

Revision History

<table>
<thead>
<tr>
<th>Document</th>
<th>Carrier</th>
<th>Rev</th>
<th>Date</th>
<th>Approved By</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1.0</td>
<td>INITIAL</td>
<td>15/11/2020</td>
<td>Leonid S.</td>
<td></td>
</tr>
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</table>
| 1.1      | 1.1     | 1) Power supplies changed to 12V in and 6A output  
2) SOM power in pins were added in place of ground.  
3) 2 Additional GPIO pins routed to MIPI-CS1 edge connector |
| 1.2      | 1.1A    | 1) RS422 RX_EN line routed to GPIO  
2) Power Jack J43 changed to 2mm instead of 2.5mm |
| 1.3      | 1.2     | 1) New layout. All previous changes implemented  
2) Change SATA lines to 100 Ohms differential  
3) M40_GPIO0_01 line moved to support PCI clock disable  
4) HDMI_RX0_HP D pull up added  
5) U31, U41 Note added. |
| 1.4      | 1.3     | 1) U34 changed to PTN36043ABXY.  
2) HDMI Out port section changed (replaced HDMI companion chip with simple ESD devices)  
3) U31, U41 changed to FPF2193  
4) R0402, C0402, TPD4EUSB30, SDC224-A Footprints changed  
5) R0603, R1210, MCHI05030-6RBM-R8 Footprints changed  
6) MA2SD290GL changed to BAS70J/FILM  
7) Q2 changed to TPS27081A  
8) Optional resistor R92 Removed  
9) R91 Changed to 49.9R  
10) UART Selection table updated for easier understanding |
| 1.5      | 1.3     | 1) J1.27, J1.29, J4.47 Pin names updated to correct GPIO number  
2) ETH1 Bypass function names updated on J3  
3) DSI_CLK_P and DSI_CLK_N swapped on J1 and J20 |
| 1.6      | 1.3     | 1) U34 changed to PTN36043BXY to reflect actual assembly  
2) U34 EOL Note added |
Please pay attention: DSI CLK P replaced by LVDS CLK N
DSI CLK N replaced by LVDS CLK P
05. ETH, uSD, AUDIO, CAN, RS422

Gigabit Ethernet1

LAYOUT NOTE:
Giga Ethernet Differential Pair, Follow Giga Ethernet routing guidelines. Differential Impedance: 100 ohms

uSD CARD

LAYOUT NOTE:
Rig external differential pairs, Follow Giga Ethernet routing guidelines. Differential Impedance: 100 ohms

CAN BUS

AUDIO

Headphones

Line In

DIGITAL MIC

RS-422 TRX

Variscite
**uHDMI IN PORT**

**LAYOUT NOTE:**
- Use HDMI and DP differential pairs for optimal performance.
- For example, pins 1 and 2 should be connected in series.

- Differential impedance: 100 ohms
- Each HDMI and DP differential signal is a pass-through on the RCLAMP0524J.
- For example, pins 1 and 8 have the same net name.

TP480USB is footprint compatible to RCLAMP0524J

**MIPI-CSI0 + MIPI-CSI1**

**LAYOUT NOTE:**
- Differential impedance: 100 ohms
- SE 50 ohms
- HS mode: DIFF
- LP mode: SEL
- Lane rate: 1.5 Gbps
- MCLK: 6-27 MHz

**NOTE:**
- I2C and GPIO run at 1.8 V

**MIPI-CSI0 + MIPI-CSI1 Connector to Variocite Custom MIPI-CSI2 CMG Board Plug in 180° to test second interface as 4 lanes

**Title**
- MIPI-CSI0 + MIPI-CSI1

**Schematic Diagram**
- Diagram showing various connections and components for HDMI, MIPI-CSI0, and MIPI-CSI1 interfaces.

**Legend**
- Various symbols representing components such as resistors (R), capacitors (C), and other electrical elements.

**Variscite Logo**
- Variscite logo appears at the bottom right of the page.
**LAYOUT NOTE:**

Differential Impedance: 100 ohms

**HDMI POWER**

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**HDMI OUT PORT**

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**DP PORT**

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**HDMI/eDP/DP SWITCH**

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Please pay attention:

- DP Lane 0 is HDMI Lane 2
- DP Lane 2 is HDMI Lane 0

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Note: HDMI pull down must not be applied until VDD_PHY_1V8 is up. Implementation uses fact that BASE_PER_3V3 rises after all SOM power rails are up. At boot time GPIO drives U57 switch to A state.

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7. HDMI, eDP Out

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Project: VAR-SP8CustomBoard 1.2

Approved By: Designer: Leonid S.

Sunday, November 01, 2020

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Variscite

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08. PCIe, uSATA

SATA 3.0

LAYOUT NOTE:
- Place AC caps close to the connector.
- SATA Differential Pair, Follow SATA routing guidelines.
- Differential Impedance: 100 ohms
- Length match +/- 5 mil.

PCIe CLOCK DIST.

LAYOUT NOTE:
- Place parallel termination resistors close to the SOM connector as possible.

Custom board 5V power supply is limited to 3A, shared with board's USB and SATA devices. Do not connect devices which exceed current limitation.

mPCIexp

LAYOUT NOTE:
- Place parallel termination resistors close to the connector.
- Differential Impedance: 100 ohms
- Length match +/- 5 mil.

Variscite
12. USB 3

USB TYPE C CIRCUITRY

USB3 SIGNALS

5V Source Load Switch

Config Channel Logic Detection & Indication of Plug Orientation

NOTE FOR U34:
P/N PTN36043BXY is EOL; New designs should include PTN36043ABXY

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

USB Profile 1 = 5 V @ 2 A: 1 A current limitation due to system power limitation of CPU Card + Base Board.
### 14. PINMUX J1 & J2

<table>
<thead>
<tr>
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<th>ALT1</th>
<th>ALT2</th>
<th>ALT3</th>
<th>CR_FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Pinmux J1 & J2**

- **Function Descriptions**
  - CB_FUNCTION
  - LSIO.GPIO0.IO16: GPT0_COMPARE
  - LSIO.GPIO0.IO17: GPT1_CLK(I2C2_SCL)
  - LSIO.GPIO0.IO18: GPT1_CAPTURE(I2C2_SDA)
  - LSIO.GPIO0.IO19: GPT1_COMPARE(GPIO0_IO19)
  - LSIO.GPIO0.IO20: UART0_RX
  - LSIO.GPIO0.IO21: UART0_TX
  - LSIO.GPIO0.IO22: UART0_RTS_B
  - LSIO.GPIO0.IO23: UART0_CTS_B
  - LSIO.GPIO0.IO24: UART1_TX
  - LSIO.GPIO0.IO25: MIPI.CSI0.I2C0_SCL
  - LSIO.GPIO0.IO26: MIPI.CSI0.I2C0_SDA
  - LSIO.GPIO0.IO27: MIPI.CSI0_SSI_SCL
  - LSIO.GPIO0.IO28: MIPI.CSI0_SSI_SDA
  - LSIO.GPIO0.IO29: MIPI.CSI1_SSI_SCL
  - LSIO.GPIO0.IO30: MIPI.CSI1_SSI_SDA
  - LG64_GPIO2_GPIO0.IO01: LVDS1_GPIO01(GPIO1_IO11)
  - LG64_GPIO2_GPIO0.IO02: LVDS1_GPIO00(GPIO1_IO12)
  - LG64_GPIO2_GPIO0.IO03: LVDS1_GPIO03(GPIO1_IO13)
  - LG64_GPIO2_GPIO0.IO04: LVDS1_GPIO04(GPIO1_IO14)
  - LG64_GPIO2_GPIO0.IO05: LVDS1_GPIO05(GPIO1_IO15)
  - LG64_GPIO2_GPIO0.IO06: LVDS1_GPIO06(GPIO1_IO16)

- **Additional Details**
  - **Project:** VAR-SP8CustomBoard
  - **Date:** Tuesday, September 01, 2020
  - **Approved By:** Leonid S.
### 15. PINMUX J3 & J4

<table>
<thead>
<tr>
<th>ALT0</th>
<th>ALT1</th>
<th>ALT2</th>
<th>ALT3</th>
<th>CR_FUNCTION</th>
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<tbody>
<tr>
<td>ENET0_MDC</td>
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<tr>
<td>ENET0.MDC1</td>
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<td>ENET0.MDC4</td>
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<td>ENET0.MDC4</td>
<td>ENET0_MDC</td>
<td>ENED_GPIO2.10</td>
</tr>
</tbody>
</table>

**Pin Multiplexing**

- **PINMUX J3**
- **PINMUX J4**

**Alt0, Alt1, Alt2, Alt3**

<table>
<thead>
<tr>
<th>CB_FUNCTION</th>
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<td>ENET0.MDC1</td>
<td>ENET0.MDC1</td>
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<td>ENET0.MDC4</td>
<td>ENET0.MDC4</td>
<td>ENET0.MDC4</td>
</tr>
</tbody>
</table>

**Function Assignments**

- **ENET0.MDC1**
- **ENET0.MDC2**
- **ENET0.MDC3**
- **ENET0.MDC4**

**Other Function Assignments**

- **USB.SDIO.SDO**
- **USB.SDIO.SDI**
- **USB.SDIO.TX**
- **USB.SDIO.RX**
- **USB.HSIC0.STROBE**
- **USB.HSIC0.DATA**
- **USDHC1.CMD**
- **USDHC1.DAT**
- **USDHC1.DATA**
- **USDHC1.RESET.B**
- **USDHC1.RESET.B**

**Component Assignments**

- **VAR-SP8CustomBoard**
- **VAR-SP8CustomBoard**
- **VAR-SP8CustomBoard**

**Design and Revision Details**

- **Approved By:**
- **Designer:**
- **Project:**
- **Date:**
- **Sheet:**

---

**Additional Notes**

- **ENET0.REFCLK.125M.25M**
- **ENET0.PPS**
- **USB_HSIC0_STROBE**
- **USB_HSIC0_DATA**
- **AUD.ESAI1.TX4.RX1**
- **AUD.ESAI1.TX3.RX2**
- **M40.GPIO0.IO03**
- **M40.GPIO0.IO00**
- **M41.GPIO0.IO00**
- **AUD.SAI0.RXD**
- **AUD.ESAI1.TX1**
- **AUD.ESAI1.TX2.RX3**
- **AUD.ESAI1.TX3.RX2**
- **MLB.CLK**
- **MLB_DATA**
- **USB.HSIC0.RDY**
- **USB.HSIC0.RST**
- **USB.SDIO.SDA**
- **USB.SDIO.SCL**
- **USB.SDIO.PWR**
- **USB.HSIC0.RDY**
- **USB.HSIC0.RST**
- **USB.SDIO.SDA**
- **USB.SDIO.SCL**
- **USB.SDIO.PWR**

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**Diagram Details**

- **Variscite**
- **Logo**
- **Document Number**
- **Rev**
- **Variscite**