**Revision History**

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<td>Revised</td>
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<td>1.2</td>
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<td>Added SW1 icon short symbol</td>
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<td>Updated compatibility values for SOM pins 64,69,176</td>
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<td>Updated SOM pin 26 net name</td>
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<td>1.3</td>
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<td>1.2</td>
<td>Changed R123 to R127 to N.C.</td>
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<td>Changed R123 to R127 to N.C.</td>
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<td>Added resistors R130-132</td>
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<td>Updated var-socket VAR-SOM-MXxx Symbol</td>
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<td>Updated PCB resistance value</td>
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**Disclaimer:**

Schematics are for reference only. Variscite LTD reserves the right to modify the use of these schematics. Schematics are subject to change without notice.
Differential Impedance: 100 ohms

LAYOUT NOTE:
Place parallel termination resistors as close to the SOM connector as possible.

SOM & U. NAND signals should not be driven.

FOR SOM-MX6 using internal SoC clock:
install 100nF instead of R37, R38
remove R22, R23, R35, R36

R22, R23, R35, R36 assembled with Ferrite Bead P/N: BLM15BA330SN1D for EMI suppression

mPCIexp

Place AC caps close to the connector

LAYOUT NOTE:
PCIE Differential Pairs. Follow PCIe routing guidelines.
Differential Impedance: 85 ohms
Length match +/-5mil

PCIe CLK

Note:
1. Default always ON. To disable clock install R21.
2. Replace PN: AB-557-03-HCHC-F-L-C
3. Disabled with SW6 in ON state

Differential Impedance: 100 ohms

LAYOUT NOTE:
Place parallel termination resistors close to the mPCIe connector

PCIe#A_DIS_B TP1

Reserved U. C8 GND
Reserved U. C4_Disables
GND3 PERST
PER0
GND6 USB D
GND12 LED PWAN
Reserved08 1.5V 2
Reserved09 GND7
Reserved10 3.3V 2
10. Debug, GPIO Exp, Buttons, LED

**USB UART DEBUG**

- USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
- Length Match: +/- 100 mils
- Differential Impedance: 90 ohms

**GPIO EXPANDER**

- In VAR-SOM-MX8 SOM pin 29 EXP_INT is referenced to 1.8V. When using pin 29 as an input pin driven by higher input voltage, use an external voltage divider to limit the current using a series resistor to a maximum of 1mA.

**GP BUTTON**

- EXP_SW1
- EXP_SW2
- EXP_SW3

**GP LED**

- EXP_LED

**VARISCITE**

Variscite logo and branding information.
11. LVDS, DSI, Touch

RESISTIVE TOUCH

CAPACITIVE TOUCH

LVDS DISPLAY A

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

LVDS DISPLAY B

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

MIPI DSI DISPLAY

LAYOUT NOTE:
LVDS Differential Pair, Follow LVDS routing guidelines. Differential Impedance: 100 ohms

Note: It is recommended to add placeholders for common mode chokes/ferrites on the LVDS lines for improvement of EMI suppression.

Short circuit protection

See note in "Headers" Page 14

Note: Please see note on Headers page regarding Touch interrupt.

Variscite
USB2 Host

LAYOUT NOTE:
USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines.
Length Match: +/- 100 mils
Differential Impedance: 90 ohms

NOTE:
Power always enabled; in order to control the power see page 14 "Headers"
14. Headers

Headers arranged for compatible alternate function

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<td>UARTRX</td>
<td>UARTRX</td>
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<td>UARTTX</td>
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<td>PWM#B</td>
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Headers arranged for partial compatible alternate function

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<th>UART/QSPI</th>
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<tr>
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<td>UARTRX</td>
<td>SPISDI</td>
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I2C A has internal pulls in Camera buffer
I2C B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Located on PS

MX6/SOLO: PIN68 WDOG1_B
SOM_6UL: PIN57 WDOG1_B

See J3.12

UART/QSPI

SAI/SPI

For complete header alternate function refer to "VAR-SOMs_Compatibility_and_Pinout.XLS" located at: ftp://ftp.variscite.com/SOM_Compatibility