

Symphony-Board



### CONTENT

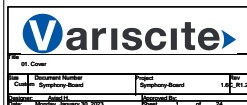
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### Disclaimer:

Schematics are for reference only.  
Variscite LTD provides no warranty for the use of these schematics.  
Schematics are subject to change without notice.

### Revision History

Document	Carrier	
1.0	1.0	Initial
1.1	1.1	Released
1.2	1.1	Updated Block Diagrams Added SH1 wire short symbol Updated Compatibility value for SOM pins 68,69,176 Updated SOM pin 22 net name Fixed U22.B1, C113.1 net name Fixed R1-R2,R35-R38 net name
1.3	1.2	Removed SH1 wire short, J1.68 routed to capacitive touch Changed R29 to C185 Changed R123,R127 to N.C. Added resistors R130-132 Removed ADC_INxx alternate function from VAR-SOM-MX8 Symbol Updated PCIe resistor assembly note
1.4	1.2	Updated Parallel Camera/HDMI/DP Note Fixed ETH pin names VAR-SOM-MX8X Symbol
1.5	1.2A	Disconnected R129
1.6	1.2A	Added VAR-SOM-MX8M-MINI Block Diagram and Symbol PRE-RELEASE VERSION!!!! Subject to change without notice
1.7	1.2B	Fixed VAR-SOM-MX8M-MINI Symbol Changed U29,U30,U31 to P/N: PPF2193 Changed R60 to 47K
1.8	1.2C	Update VAR-SOM-MX8M-MINI Symbol to V1.1 with side notes for v1.0B(Early access customers) Update VAR-SOM-MX8M-MINI Block Diagram POR circuitry fed by VCC_SOM: see U7 R60 R61 R40 R60 D5 Removed
1.9	1.2D	Raise VCC_3V3 to Nominal 3.39V for VAR-SOM-MX8M-MINI/NANO power up threshold voltage requirement of >3.35V
1.10	1.2E	Reference for new designs: (changes not implemented in V1.2 BRD) * Added x2 studs for heat plate support * Base_per_3v3 added slew rate limit * U7 (Base POR circuit) added CB_WDOG resistor assembly options * U29 U30 U31 - Added assembly note * VAR-SOM-MX8M-NANO pages added with symbol pinout * VAR-SOM-MX8 Connector update - added NC on /? assembly options * Power switch in OFF position discharge of Custom rails added * Ethernet magnetics - support two Marf: Pulse & UDE; * Base RJ45 LEDs matched to SOM behaviour;
1.11	1.3	* Added VAR-SOM-MX8M-PLUS Preliminary Symbol and Block Diagram Symbol is Pre-Release Version! Subject to change without notice! * All C1210 capacitor footprint updated to C1210_v0 * MS1 to MS6 not assembled
1.12	1.3A	* ETH1 PHY clock filter U9 replaced with 49.5 Ohm /0603 resistor * Added design note for ETH1 switches U8 and U10.
1.13	1.4	* MS5 and MS6 location adopted to heatplate design - Layout * Update J1 Manufacturer P/N, NAME and footprint to represent the assembled part * Replace PCIe AC caps on RX lines with 0 ohm resistors * Updated VAR-SOM-MX8M-PLUS Symbol pins 1 58 80, swap pins 41 43 and 84 147 * J19 Modify Camera connector orientation * Remove U8 U10 analog switches on ETH1 * U9 revert to EMI filter on RGMII_RX clock line * Added RN1 RN2 RN3 R151 R136 isolating stubs on ETH1 RGMII signals * U26 footprint updated to DS * Y1 C68 C67 updated * Support for VAR-SOM-6UL boot: - BOOT_MODE1 - R117 assembled - BOOT_MODE0 - Added PD R149 - USB& PWR to HOST J23 always enabled * Remove R39 on pin J1-156 to support SOM-MX8MP 2nd MIPI-CSI Lane2 routing * J3 J30 pinout change
1.14	1.4A	* Support for VAR-SOM-MX8MP USB OTG - Changed U5.P4 Pull for board identification, U21.9 connected to GPIO: - Changed R43,R130,R106 to N.C. - Changed R44,R132 to Assembled  * Changed Q4 P/N from: TPS27082L (EOL) to -> TPS27081A * Updated VAR-SOM-MX8M-PLUS Block Diagram, Symbol pins 36,38 names * Added notes for SOM pins 29,79,84
1.15	1.4A	Changes in v1.14/1.4A for R43,R44 were not implemented (part of board identification) and only appear in revision history; board identification implemented via EEPROM U3. Board identification required for OS to identify method of OTG ID used: PTN5150 or GPIO
1.16	1.5	* Modified VCC_3V3 to 3.35V nominal for all SOMs. For VAR-SOM-MX8M-MINI/NANO, power up threshold voltage requirement of >3.35V is implemented using Q10,R152  * Added note for VAR-SOM-MX8M-MINI/NANO pin 91
1.17	1.5	* Updated note for I2C#B pull up resistors
1.18	1.5	* Updated note for PTN36043BXY chip
1.19	1.5A	* Q10 changed to ZN7002P.Z15 Transistor Q10 changed to ZN7002P to stabilize the SOM voltage in the OFF state. Old transistor leakage current (IDG) changed the feedback current and increased the SOM voltage. ZN7002P does not have SG diode that allowed IDSS to flow into the Gate  * SOM Pin 84 Note changed
1.20	1.6	Ethernet PHY replaced to ADIN1300 R22,R23,R35,R36 assembled with Ferrite Bead C185 assembled with 10K resistor, R30 not assembled U2 changed to CBTL02043B USB3 crossover switch changed to CBTL02043B
1.21	1.6A	Due to EOL: U35 changed to NFL18ZT207H1A3D Due to allocation problems: U13 changed to SN65HVD232QDR
1.22	1.6B	Due to allocation problems: U22,U29,U30,U31 changed to P/N: PPF2194
1.23	1.6C	Added VAR-SOM-AM62 Block Diagram and Symbol Added VAR-SOM-MX93 Block Diagram and Symbol Temporary removed compatibility notes Added hand wired EXP_MDIO_EN line.



## 03.SOM

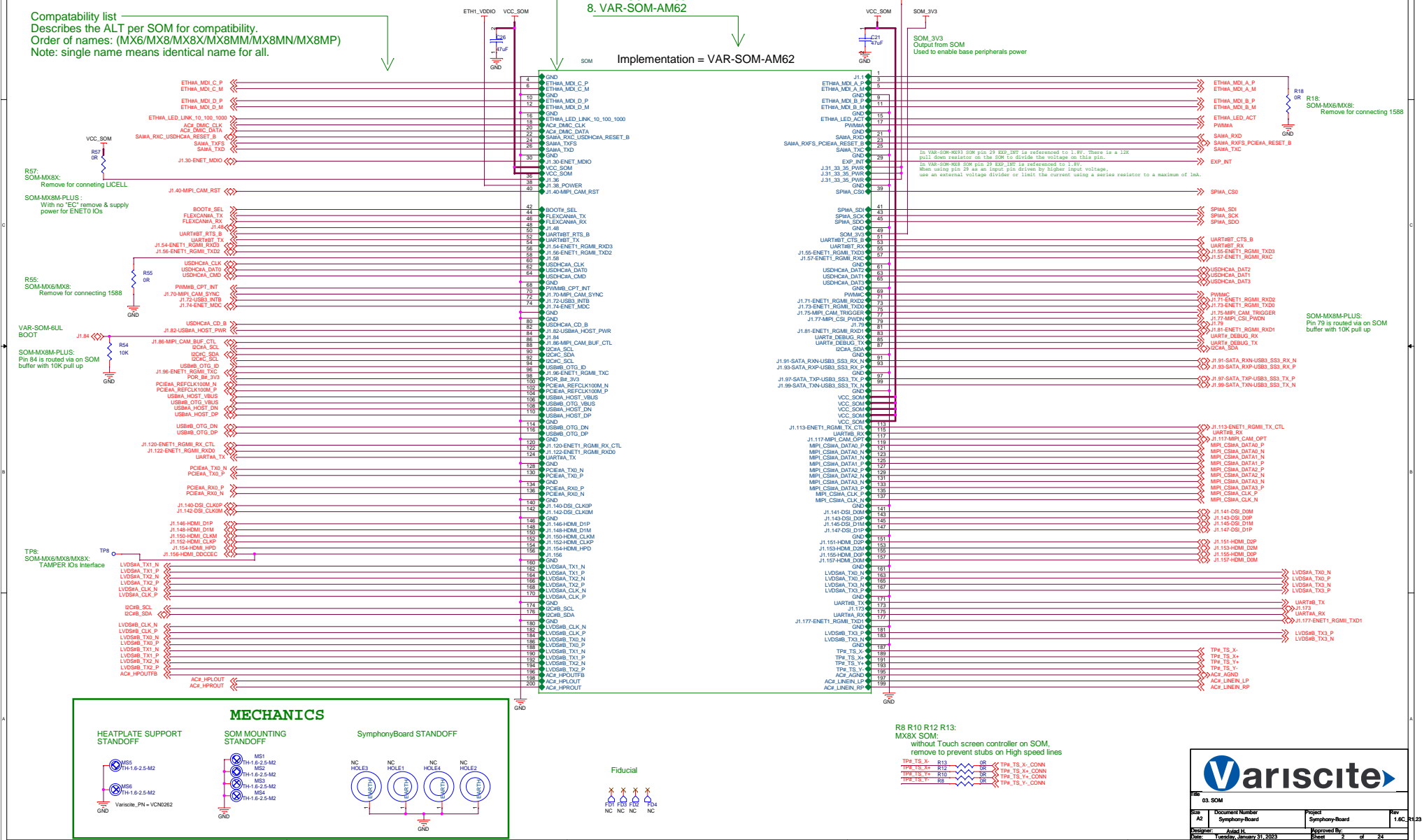
For cross probing between SOM symbol and the specific SOM Connector used, set the "Implementation" property value in SOM port symbol to one of the following:

For complete alternate function per pin and specific SOM:  
please refer to "VAR-SOMs\_Compatibility\_and\_Pinout.XLS " located at:  
[ftp://ftp.variscite.com/SOM\\_Compatibility](ftp://ftp.variscite.com/SOM_Compatibility)

OFF PAGE CONNECTOR INDEX:

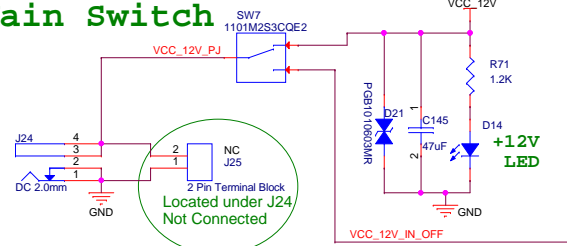
1. Function# :Interface common to ALL SOMs  
2. J1.xxx-Function :Interface common to certain SOMs or Used for carrier board common function  
3. J1.xxx :No common interface

**Compatibility list** —  
Describes the ALT per SOM for compatibility.  
Order of names: (MX6/MX8/MX8X/MX8MM/MX8MN/MX8MP)  
Note: single name means identical name for all.

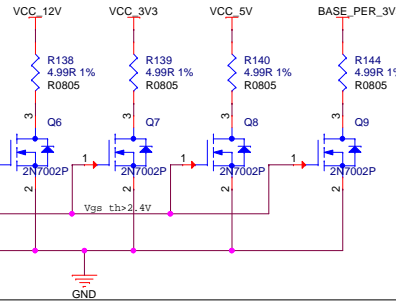


# 05. Power, Reset, Boot, RTC, EEPROM

## 12VDC INPUT Main Switch

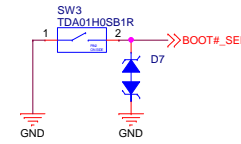


## POWER DISCHARGE

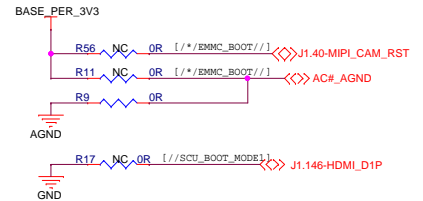


## SOM BOOTSTRP

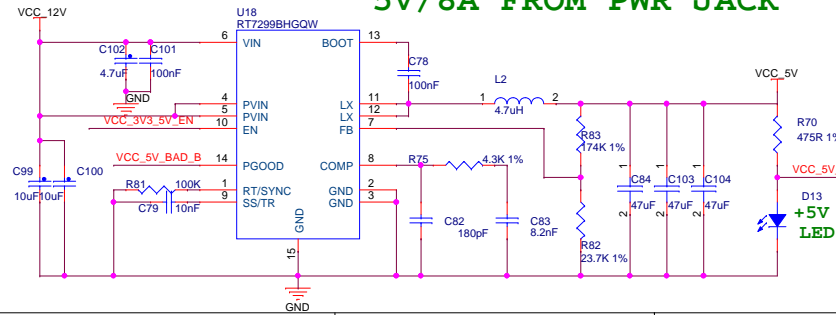
Boot Options:  
OFF : INT  
ON : SD  
Internal boot is from eMMC  
MX6 for eMMC boot see additional changes note



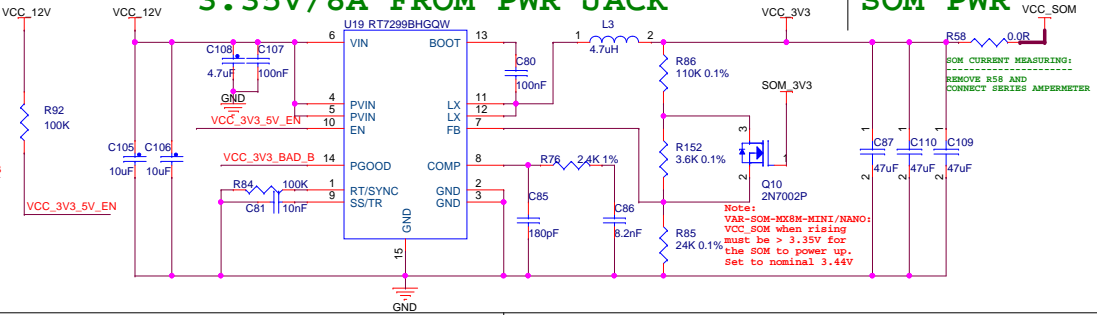
For supporting MX6 eMMC boot option:  
Remove R9  
Assemble R56,R11  
Note: Normal configuration is with NAND



## 5V/8A FROM PWR JACK



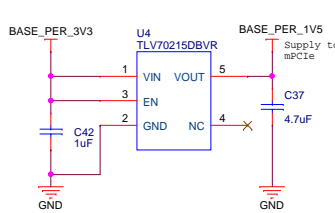
## 3.35V/8A FROM PWR JACK



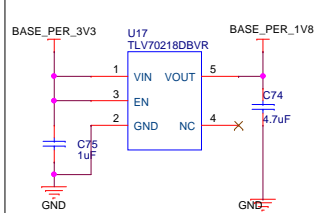
## SOM PWR

SOM CURRENT MEASURING:  
REMOVE R58 AND  
CONNECT SERIES AMPERMETER

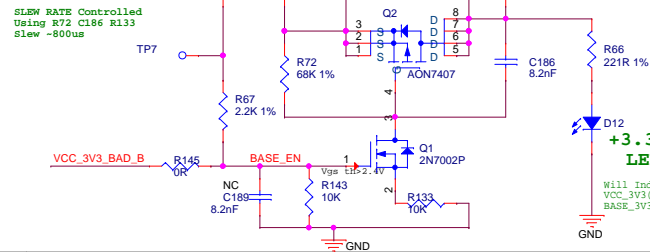
## 1.5V BASE



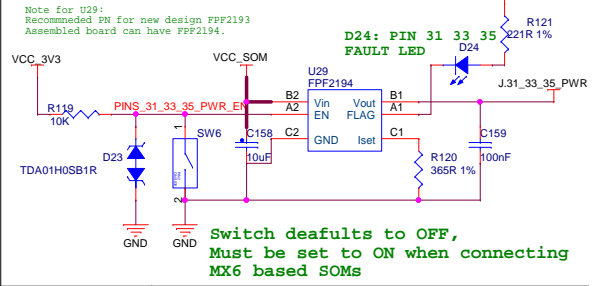
## 1.8V BASE



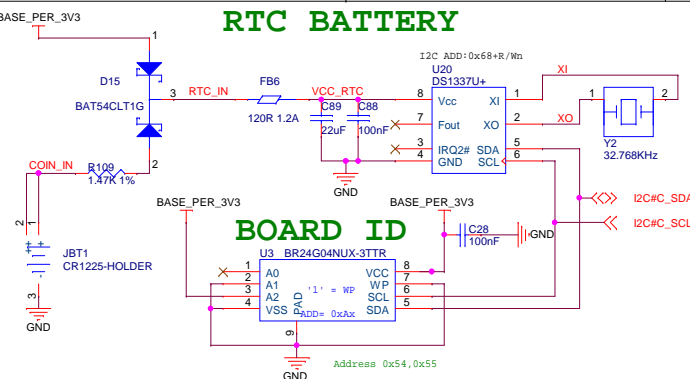
## BASE\_3V3



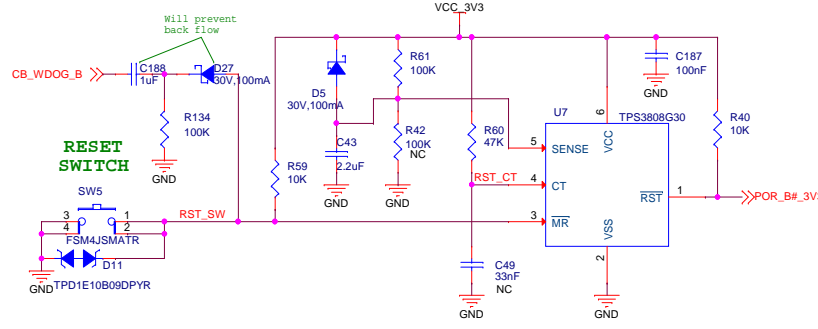
## PINS 31 33 35 POWER



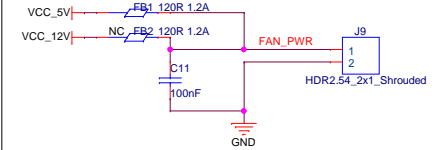
## RTC BATTERY



## RESET CIRCUITRY



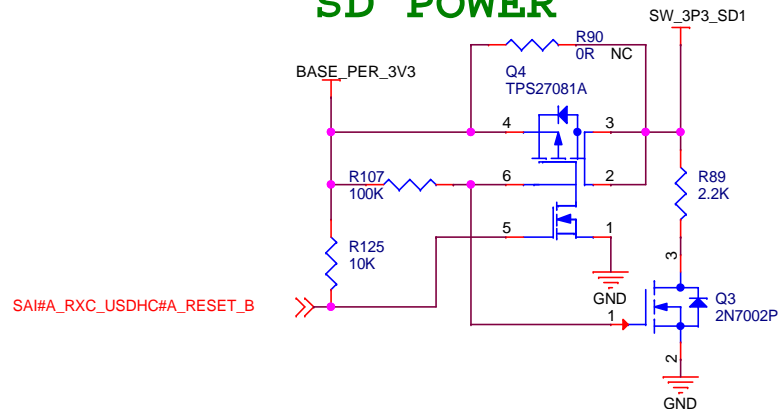
## FAN PWR



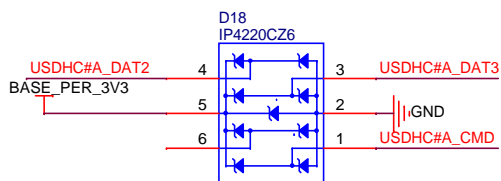
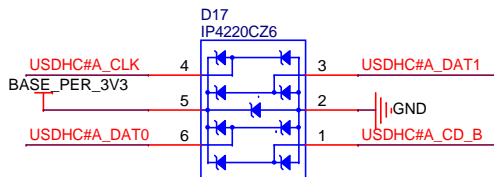
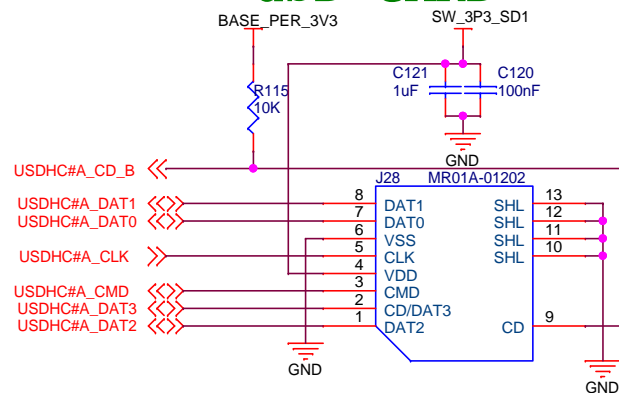
Title 05. Power,Reset,Boot,RTC,EEPROM			
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Designer Aviad H.	Approved By:		
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# 06. uSD, Audio,CAN

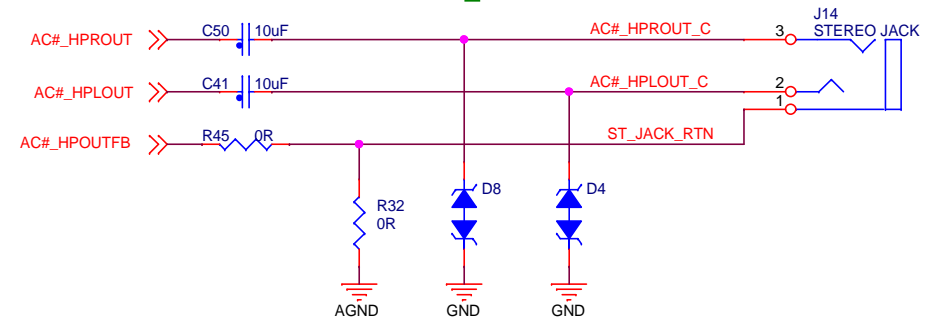
## SD POWER



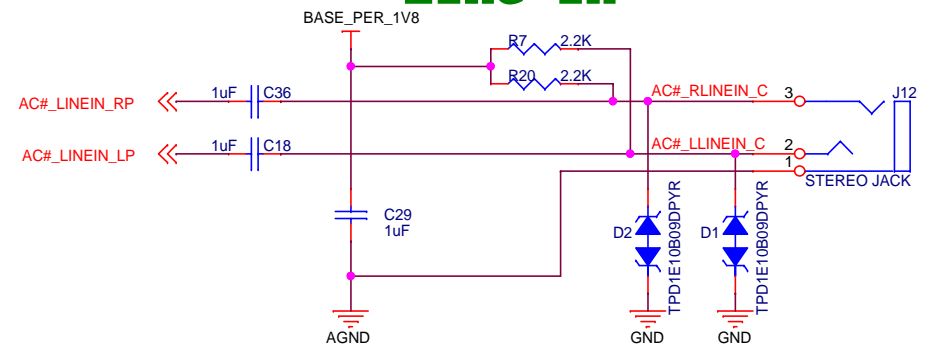
## uSD CARD



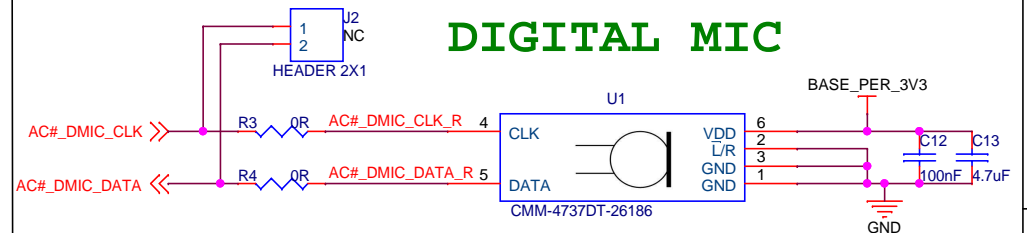
## Headphones



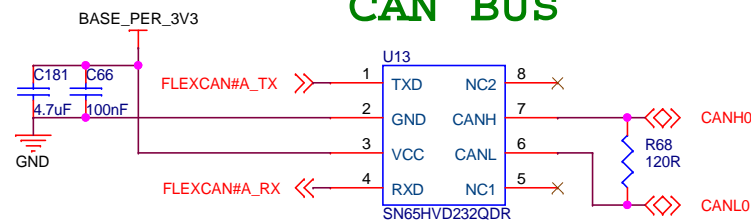
## Line In



## DIGITAL MIC

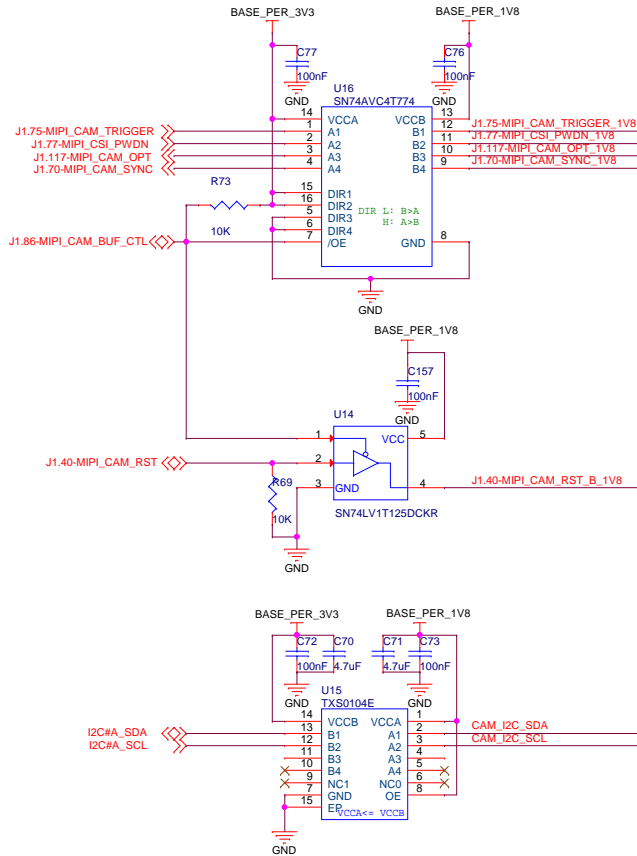


## CAN BUS

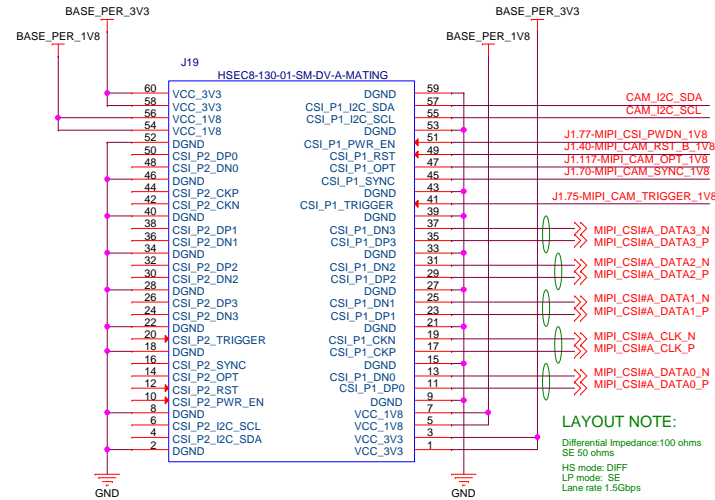


Title 06. uSD, Audio,CAN			
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## 07. Camera, HDMI, DP



## MIPI-CSI



### LAYOUT NOTE:

Differential Impedance: 100 ohms  
SE 50 ohms  
HS mode: DIFF  
LP mode: SE  
Lane rate: 1.5Gbps

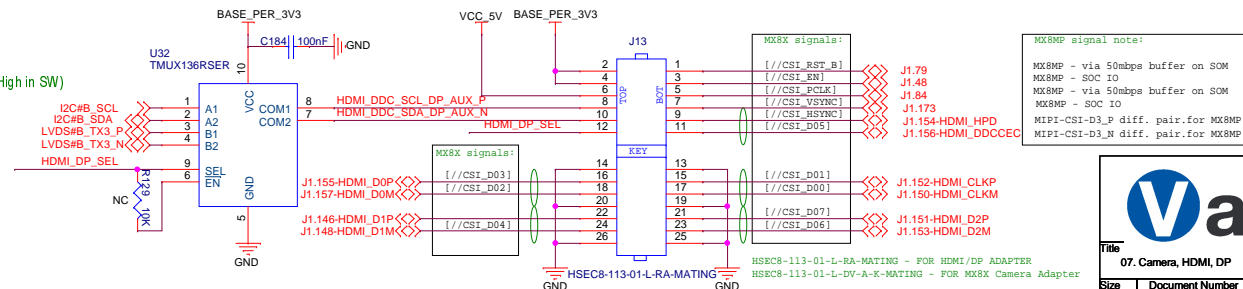
Note:  
MIPI\_CSI#A signals appears on bottom side of J19  
as of SymphonyBoard V1.4.

## J13: MX6/MX8-HDMI, MX8-DP, MX8X-CSI, MX8MP-2nd MIPI-CSI

Note for U32 (analog switch):  
Switch is to enable support for the following adapters:  
Parallel camera, HDMI, DisplayPort and second MIPI-CSI.

- Switch select controlled on adaptor will select between:  
1) I2C#B which can export  
VAR-SOM-MX8X: I2C3 Used by parallel camera  
VAR-SOM-MX8: HDMI DDC Used by HDMI (GPIO1\_22 in should be set High in SW)  
2) LVD#B\_TX3 which can export:  
VAR-SOM-MX8(DP assembly option): HDMI AUX used by DP

Switch can be omitted when designing for only one of the above interfaces.



Title 07. Camera, HDMI, DP			
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## 08. Ethernet

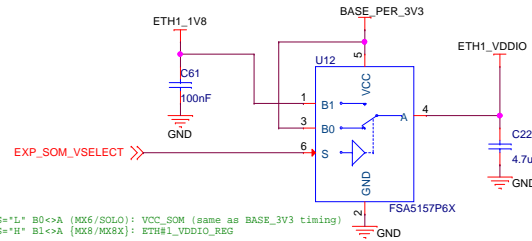
### Header/Stub isolation resistors

J1.54-ENET1_RGMII_RXD3	ENET1_RGMII_RXD3	NC	R173	0R	J1.54_EXT
J1.71-ENET1_RGMII_RXD2	ENET1_RGMII_RXD2	NC	R174	0R	J1.71_EXT
J1.122-ENET1_RGMII_RXD0	ENET1_RGMII_RXD0	NC	R175	0R	J1.122_EXT
J1.81-ENET1_RGMII_RXD1	ENET1_RGMII_RXD1	NC	R176	0R	J1.81_EXT
J1.120-ENET1_RGMII_RX_CTL	ENET1_RGMII_RX_CTL	NC	49.9R 1%	R151	J1.120_EXT
J1.57-ENET1_RGMII_RXC	ENET1_RGMII_RXC	NC	1.0K 1%	R136	J1.57_EXT
J1.113-ENET1_RGMII_TX_CTL	ENET1_RGMII_TX_CTL	NC	R179	0R	J1.113_EXT
J1.96-ENET1_RGMII_TXC	ENET1_RGMII_TXC	NC	R180	0R	J1.96_EXT
J1.73-ENET1_RGMII_TXD0	ENET1_RGMII_TXD0	NC	R181	0R	J1.73_EXT
J1.177-ENET1_RGMII_TXD1	ENET1_RGMII_TXD1	NC	R182	0R	J1.177_EXT
J1.56-ENET1_RGMII_TXD2	ENET1_RGMII_TXD2	NC	R177	0R	J1.56_EXT
J1.55-ENET1_RGMII_TXD3	ENET1_RGMII_TXD3	NC	R178	0R	J1.55_EXT

Note:  
Customer requiring usage of J30 header (located on bottom side)  
should assemble these resistors if not assembled by default

### VDD\_ENET for SOM-MX8/MX8X/MX8MP

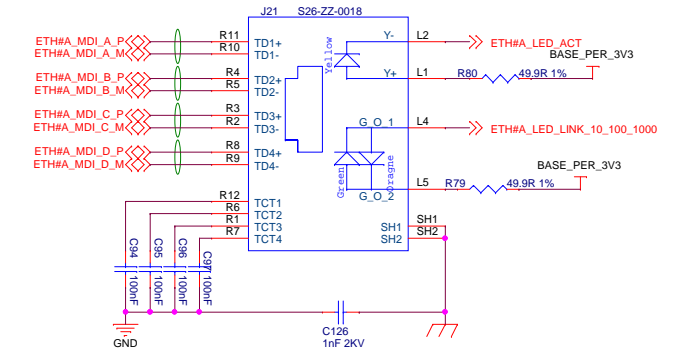
Power for ENET1\_RGMII IOs on SOM power fed from pin J1.38  
For specific SOM listed above, requiring second ETH port on ENET1 this power should be set to 1.8V source from U11 PHY



S="L" B0<A {MX8/SOLO}: VCC\_SOM (same as BASE\_3V3 timing)  
S="H" B1<A {MX8/MX8X}: ETH1\_VDDIO\_REG

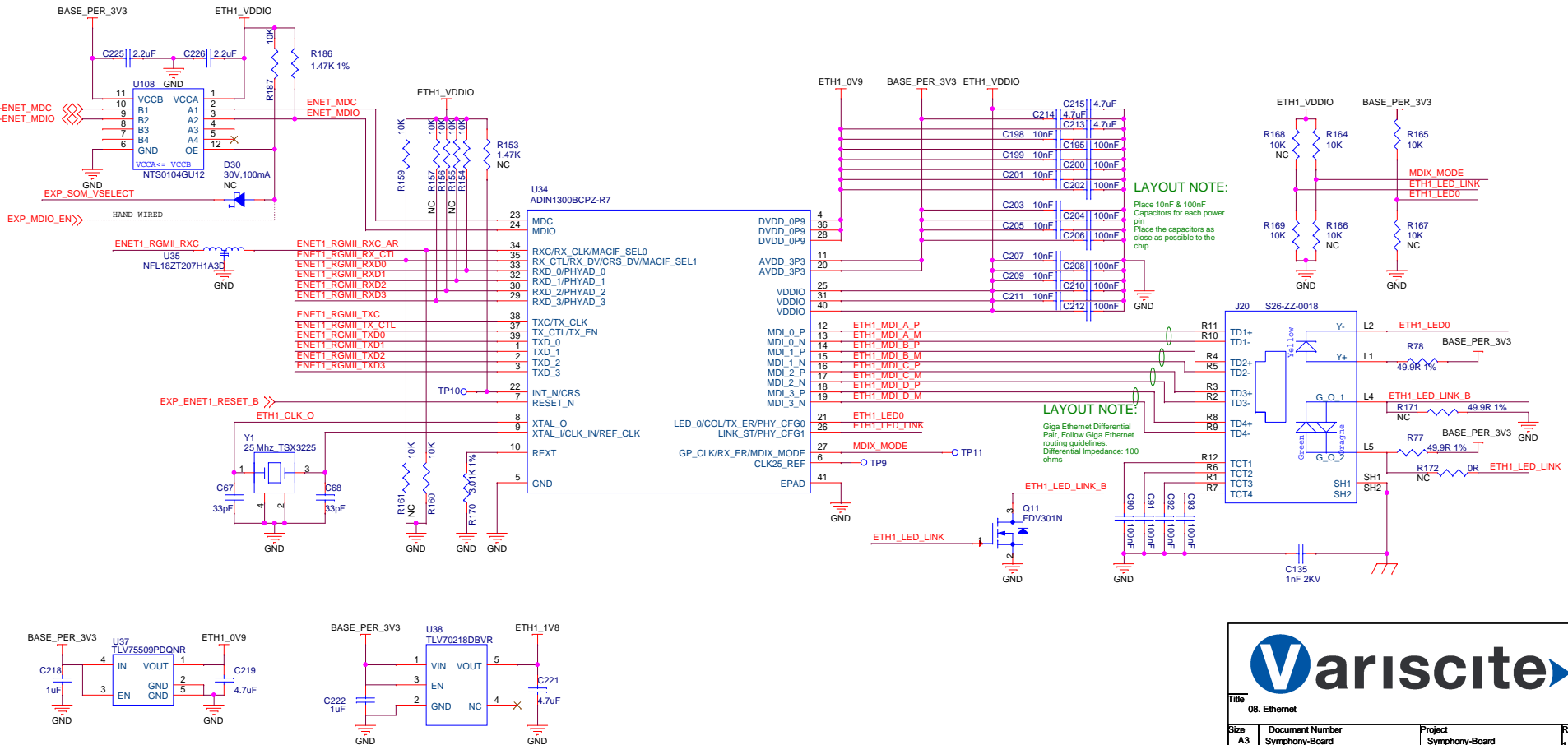
## Gigabit Ethernet (Internal)

LAYOUT NOTE:  
Giga Ethernet Differential Pair,  
Follow Giga Ethernet routing  
guidelines.  
Differential Impedance: 100 ohms



LAYOUT NOTE:  
Place 10nF & 100nF  
Capacitors for each power  
pin  
Place the capacitors as  
close as possible to the  
chip

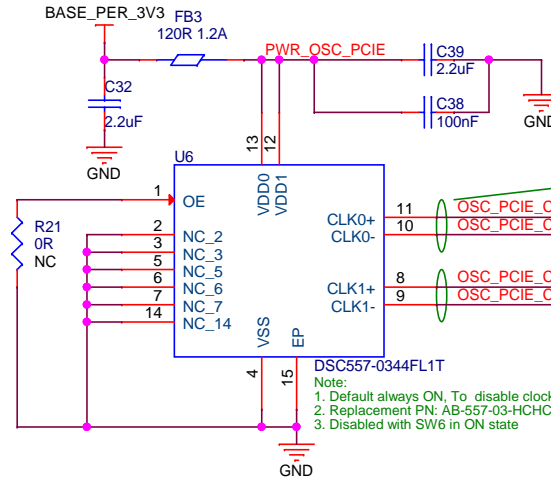
LAYOUT NOTE:  
Giga Ethernet Differential  
Pair, Follow Giga Ethernet  
routing guidelines.  
Differential Impedance: 100  
ohms



Title 08. Ethernet			
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# 09. PCIe

## PCIe CLK



### LAYOUT NOTE:

Differential Impedance:  
100 ohms

PCIE#A\_REFCLK100M\_P  
PCIE#A\_REFCLK100M\_N

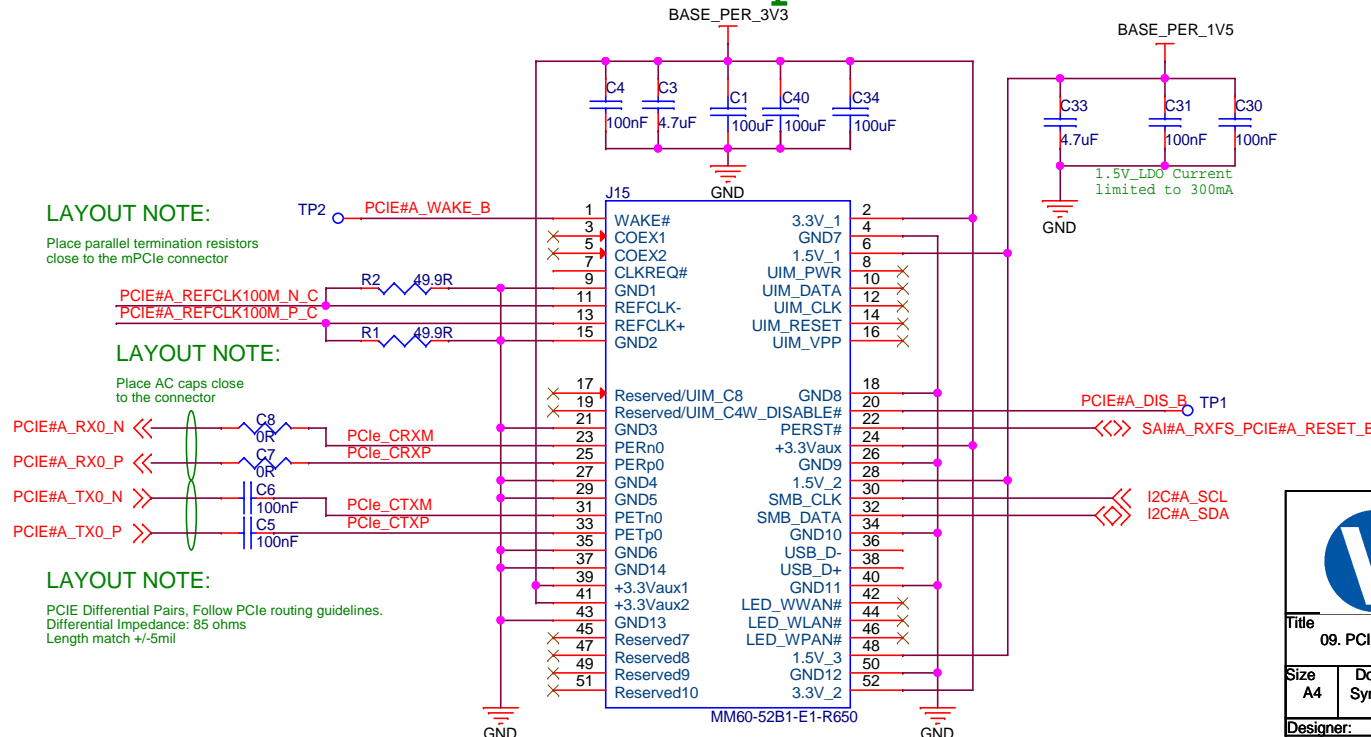
SOM-6UL NAND  
signals should  
not be driven

PCIE#A\_REFCLK100M\_P\_C  
PCIE#A\_REFCLK100M\_N\_C

### LAYOUT NOTE:

Place parallel termination resistors  
as close to the SOM connector  
as possible.

## mPCIexp



### LAYOUT NOTE:

Place parallel termination resistors  
close to the mPCIe connector

### LAYOUT NOTE:

Place AC caps close  
to the connector

### LAYOUT NOTE:

PCIe Differential Pairs, Follow PCIe routing guidelines.  
Differential Impedance: 85 ohms  
Length match +/-5mil

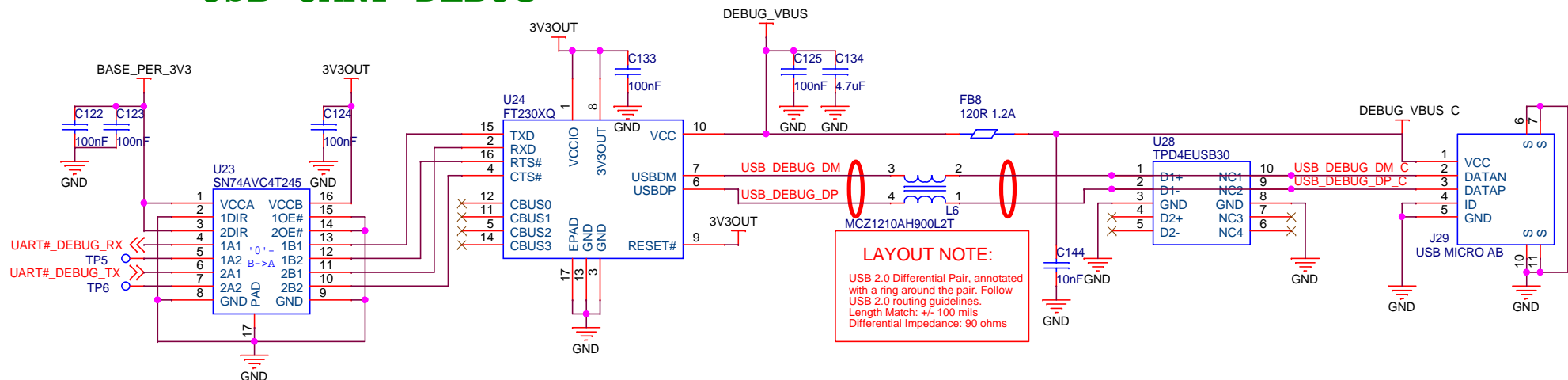


Title 09. PCIe			
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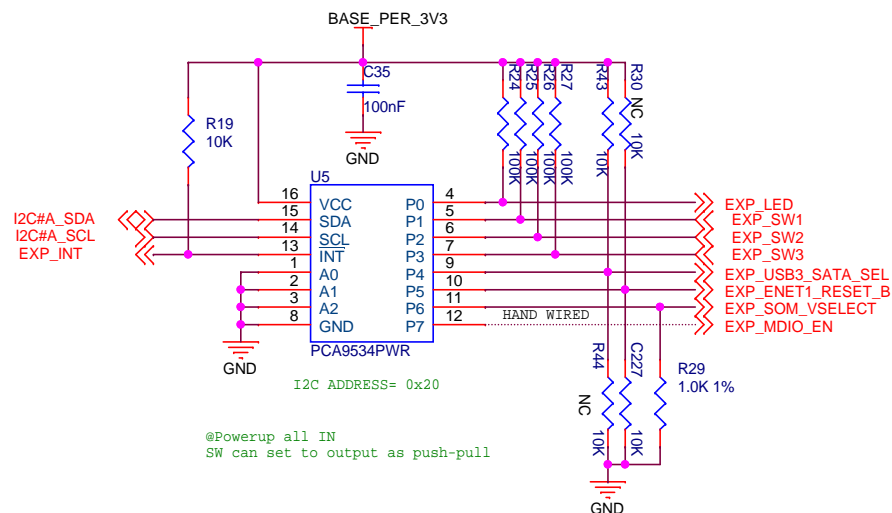


# 10. Debug, GPIO Exp, Buttons, LED

## USB UART DEBUG

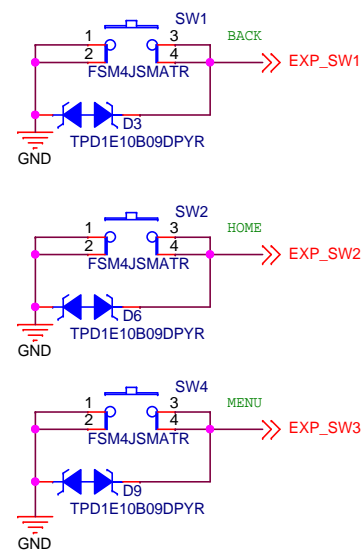


## GPIO EXPANDER



In VAR-SOM-MX8 SOM pin 29 EXP\_INT is referenced to 1.8V.  
When using pin 29 as an input pin driven by higher input voltage,  
use an external voltage divider or limit the current using a series resistor to a maximum of 1mA.

## GP BUTTON



## GP LED

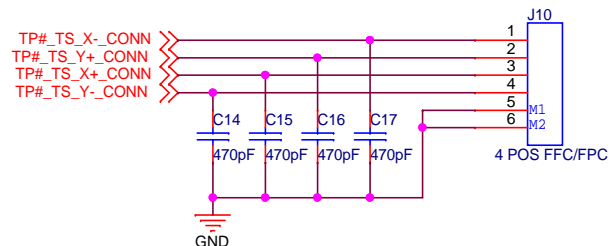


Title 10. Debug, GPIO Exp, Buttons, LED			
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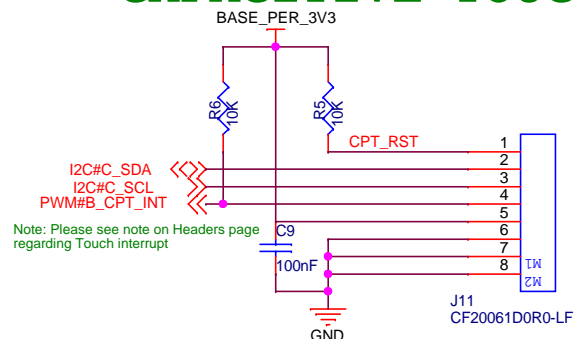


# 11. LVDS, DSI, Touch

## RESISTIVE TOUCH



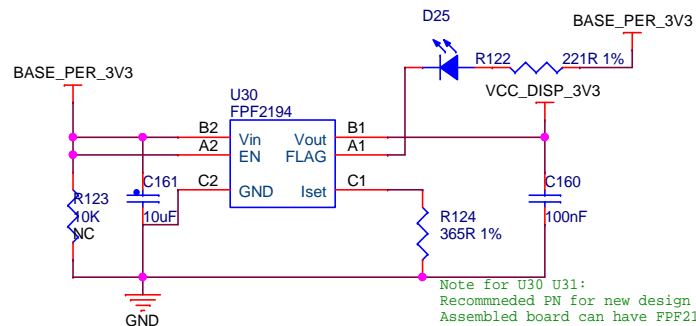
## CAPACITIVE TOUCH



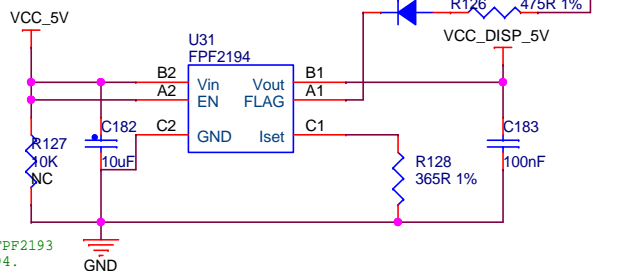
See note in :  
"Headers" Page 14

J1.57\_EXT <>>  
CB\_WDOG\_B <>>  
J1.82-USB#A\_HOST\_PWR <>>  
CB-USB#A\_HOST\_PWR <>>

## Short circuit protection



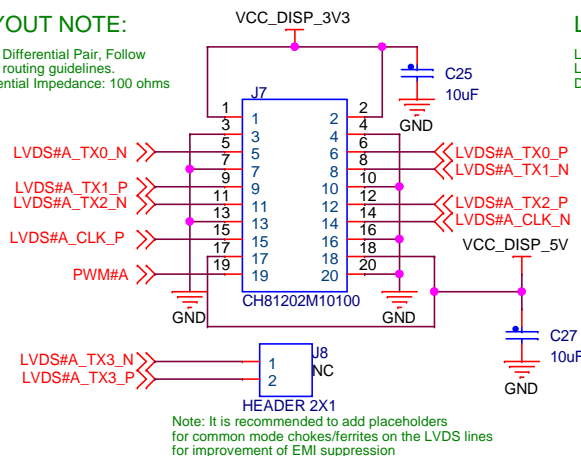
Note for U30 U31:  
Recommended PN for new design FPF2193  
Assembled board can have FPF2194.



## LVDS DISPLAY A

### LAYOUT NOTE:

LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms

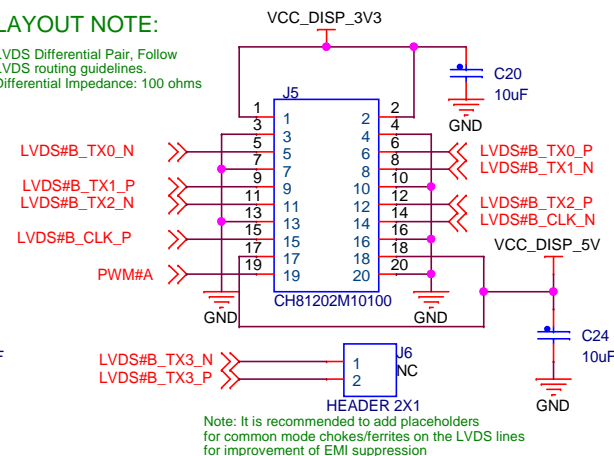


Note: It is recommended to add placeholders  
for common mode chokes/ferrites on the LVDS lines  
for improvement of EMI suppression

## LVDS DISPLAY B

### LAYOUT NOTE:

LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms



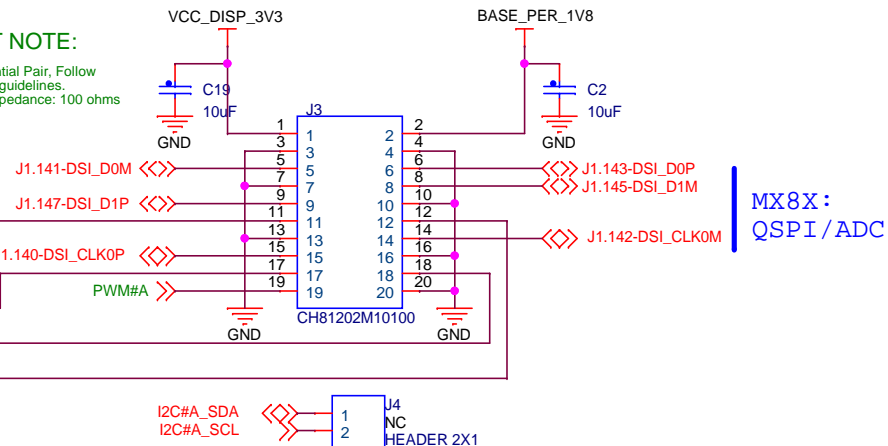
Note: It is recommended to add placeholders  
for common mode chokes/ferrites on the LVDS lines  
for improvement of EMI suppression

## MIPI DSI DISPLAY

### LAYOUT NOTE:

LVDS Differential Pair, Follow  
LVDS routing guidelines.  
Differential Impedance: 100 ohms

MX8X:  
QSPI/ADC



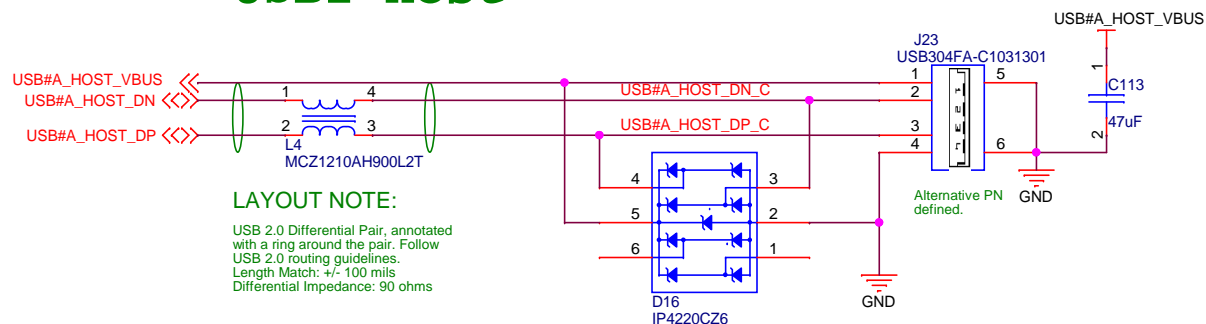
MX8X:  
QSPI/ADC



Title 11. LVDS, DSI, Touch			
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# 12. USB2 Host

## USB2 Host



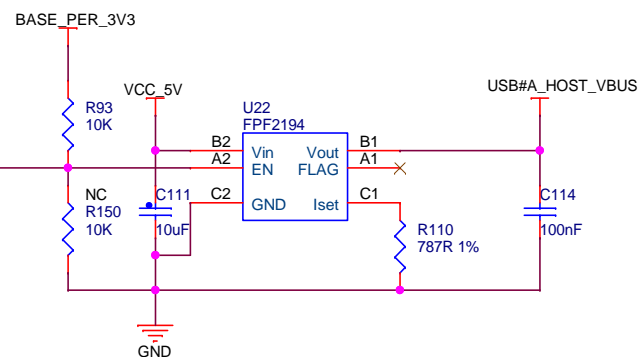
### LAYOUT NOTE:

USB 2.0 Differential Pair, annotated with a ring around the pair. Follow USB 2.0 routing guidelines. Length Match: +/- 100 mils. Differential Impedance: 90 ohms

CB-USB#A\_HOST\_PWR

### NOTE:

Power always enabled;  
In order to control the power see page 14 "Headers"



Title 12. USB2 Host			
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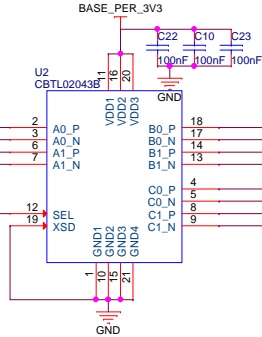
## 13. USB3, uSATA

### SATA/USB select

J1.93-SATA\_RXP-USB3\_SS3\_RX\_P  
J1.91-SATA\_RXN-USB3\_SS3\_RX\_N  
J1.97-SATA\_TXP-USB3\_SS3\_TX\_P  
J1.99-SATA\_TXN-USB3\_SS3\_TX\_N

EXP\_USB3\_SATA\_SEL >>

SEL = LOW: A <-> B  
SEL = HIGH: A <-> C  
XSD = LOW: ON  
XSD = HIGH: OFF  
By default, lines routed to SATA



#### LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 85 ohms

USB3\_SS3\_RX\_P  
USB3\_SS3\_RX\_N  
USB3\_SS3\_TX\_P  
USB3\_SS3\_TX\_N

SATA\_RXP  
SATA\_RXN  
SATA\_TXP  
SATA\_TXN

#### LAYOUT NOTE:

SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

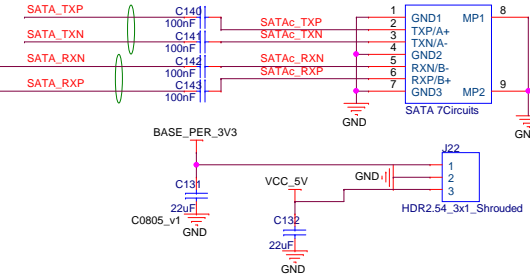
### SATA 2.0

#### LAYOUT NOTE:

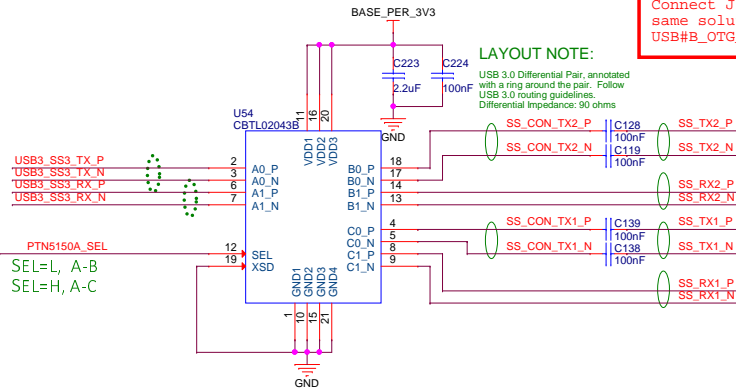
SATA Differential Pair, Follow SATA routing guidelines. Differential Impedance: 85 ohms Length match +/-5mil

#### LAYOUT NOTE:

Layout Note Place AC caps close to the connector



### USB TYPE C Circuitry



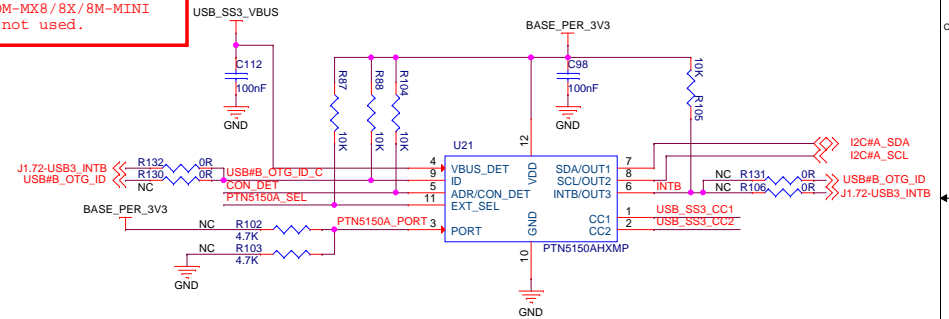
#### LAYOUT NOTE:

USB 3.0 Differential Pair, annotated with a ring around the pair. Follow USB 3.0 routing guidelines. Differential Impedance: 90 ohms

SS\_CON\_TX2\_P  
SS\_CON\_TX2\_N  
SS\_TX2\_P  
SS\_TX2\_N  
SS\_TX1\_P  
SS\_TX1\_N  
SS\_RX1\_P  
SS\_RX1\_N

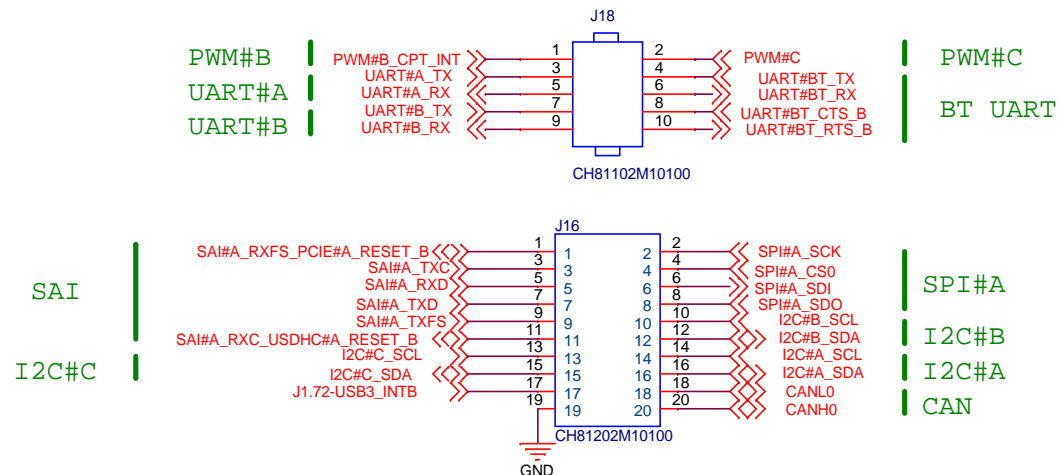
Usage of native USB\_ID for iMX8MP requires patches not included in the formal release, pull up should be to 1.8V.  
For simple OTG function for VAR-SOM-MX8M-PLUS Connect J1.72 GPIO to U22 PTN ID output - same solution applies also for VAR-SOM-MX8/8X/8M-MINI USB#B\_OTG\_ID can be left floating if not used.

### Config Channel Logic Detection & Indication of Plug Orientation

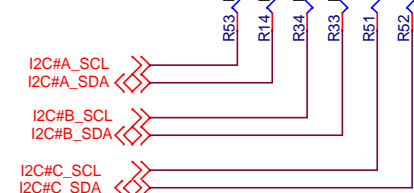


# 14. Headers

Headers arranged for compatible alternate function



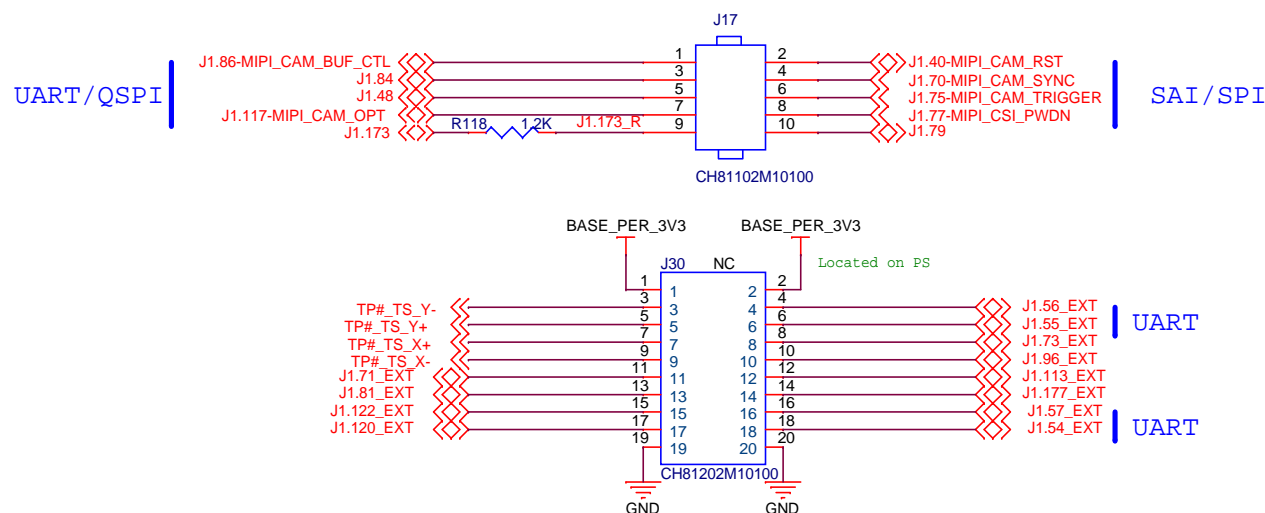
I2C PULL UPS



I2C\_A has internal pulls in Camera buffer

I2C\_B has internal pulls in MX6/MX8/MX8X/MX8MP SOMs.  
For MX8MM/MX8MN/6UL SOMs - external pull ups should be added.

Headers arranged for partial compatible alternate function



## COLD RESET ON WDOG\_B EVENT for MX6/SOLO and 6UL SOMs

Listed above SOMs require short on headers to get "reboot" to function.  
For all other watch dog looped on SOM

CB_WDOG_B	>> Symphony Board reset circuitry watch dog input	See J3.17
J1.57_EXT	<< SOM_6UL: PIN57 WDOG1_B	See J3.11
PWM#B_CPT_INT	<< MX6/SOLO: PIN68 WDOG1_B	See J18.1

## USB#A Host VBUS power control

In order to control the USB#A HOST VBUS power a short is required:  
Symphony Board U22

CB-USB#A_HOST_PWR	>> Symphony Board U22 control input	See J3.12
J1.82-USB#A_HOST_PWR	>>	See J3.18

For complete header alternate function refer to "VAR-SOMs\_Compatibility\_and\_Pinout.XLS" located at:  
[ftp://ftp.variscite.com/SOM\\_Compatibility](ftp://ftp.variscite.com/SOM_Compatibility)



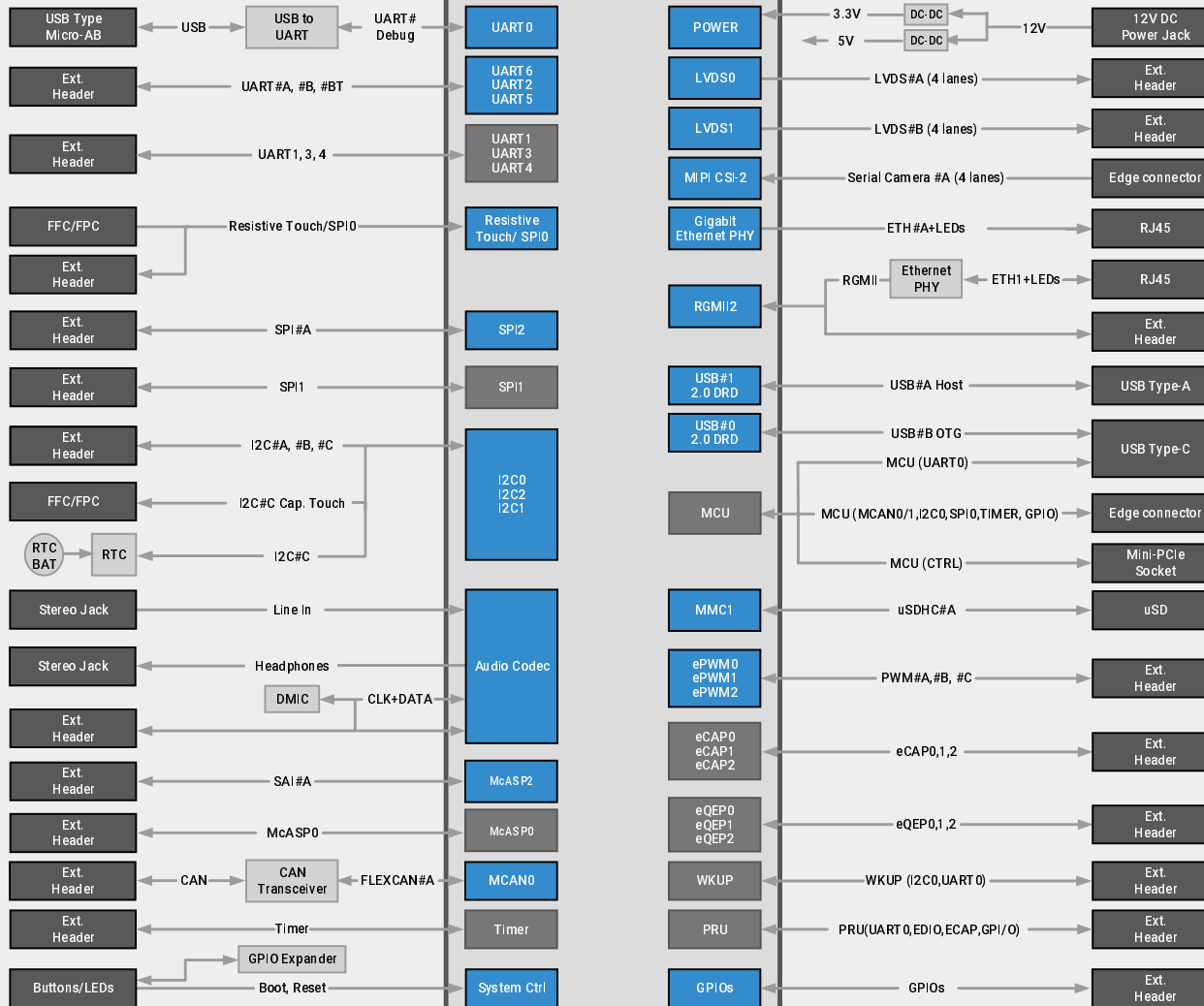
Title 14. Headers			
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## 02. Block Diagram VAR-SOM-AM62

### Symphony-Board

Doc rev 1.0

#### VAR-SOM-AM62



Pin-compatible with other modules from the VAR-SOM Pin2Pin family

No pin2pin compatibility



Title  
02. Block Diagram VAR-SOM-AM62

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04. VAR-SOM-AM62 Connector

