

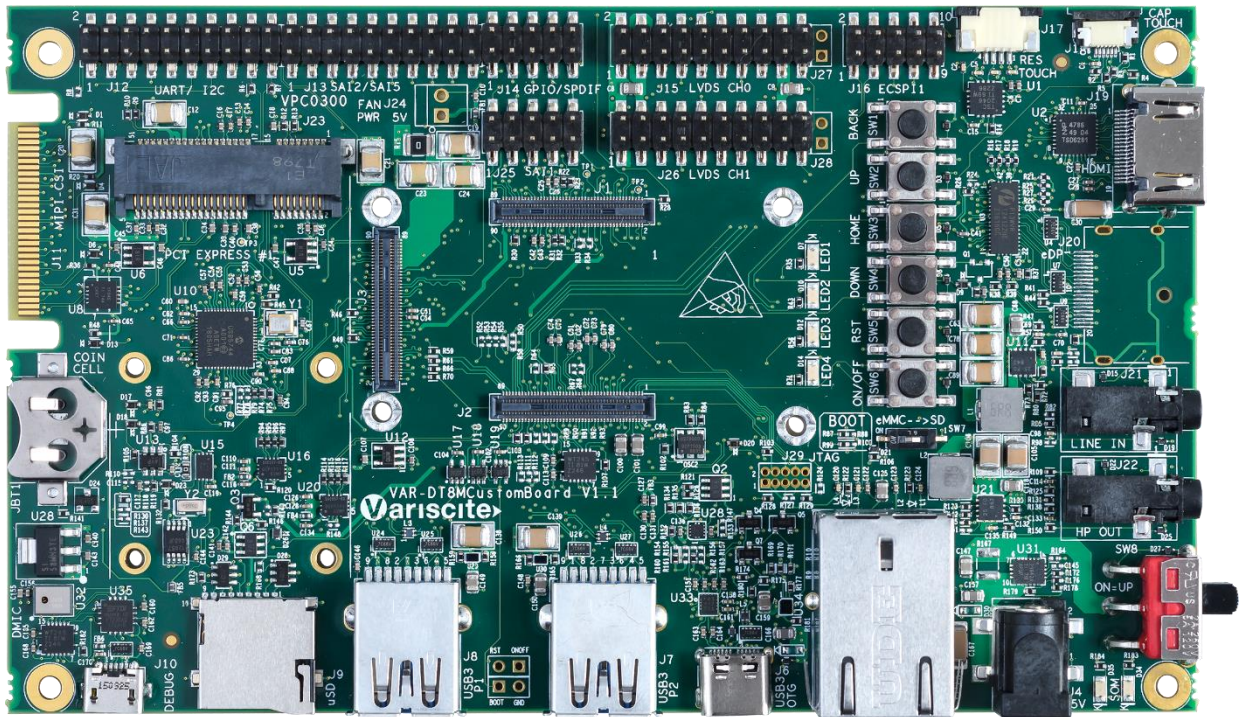


VARISCITE LTD

VAR-DT8MCustomBoard Datasheet

Carrier-board for the DART-MX8M

V 1.x



VARISCITE LTD.

VAR-DT8MCustomBoard Datasheet

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Revision History

| Revision | Date | Notes |
|----------|--------------|-----------------------|
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| 1.01 | May 13, 2018 | Official release |

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1 Overview

This chapter gives an overview of the VAR-DT8MCustomBoard.

1.1 General Information

The VAR-DT8MCustomBoard is a complete development board, utilizing all of the DART-MX8M System-on-Module's features. It is assembled with large variety of user and debug interfaces enabling it to serve as both a complete development kit or as a stand-alone end-product.

1.1.1 Supporting Variscite products

- DART-MX8M
- 7" Capacitive touch LCD

1.1.2 Supporting O.S

- Linux
- Android

1.1.3 Additional information

Board schematics as well as mechanical CAD data base is available to download at www.variscite.com,

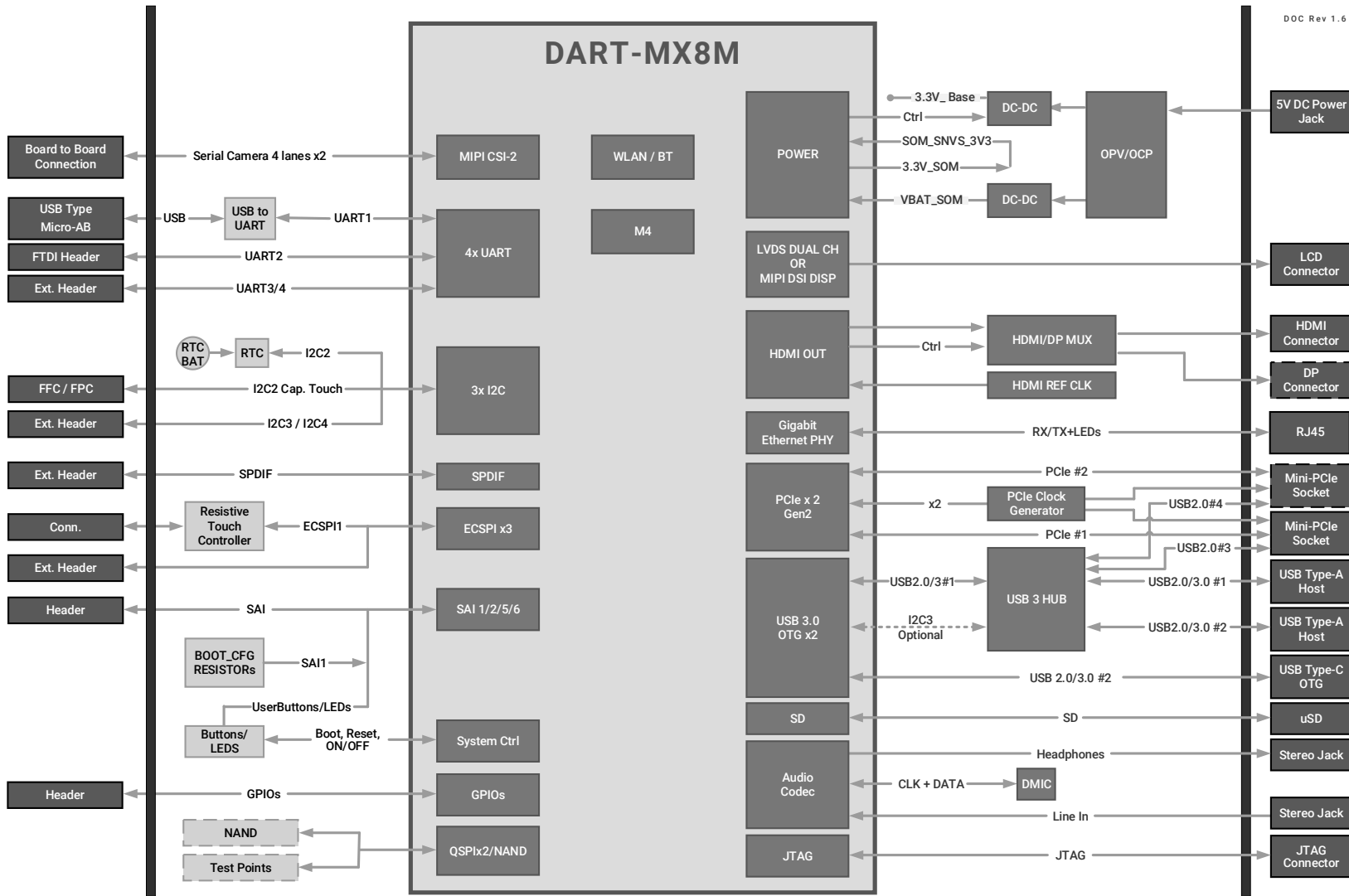
SW support information can be found: <http://variwiki.com/>

For further information contact Variscite support at <mailto:support@variscite.com>.

1.2 VAR-DT8MCustomBoard features summary

- 3 x 90 pin high density connectors, compatible with the DART-MX8M
- Display
 - 18 bit LVDS Interface supporting Variscite's 7" TFT capacitive touch LCD
 - HDMI 2.0a
 - Display Port 1.3 – **Awaits NXP release.**
- Touch panel interface
 - Capacitive - I2C based
 - Resistive – SPI based
- Ethernet
 - 10/100/1000BaseT – RJ45
- PCIe
 - Mini PCIe
 - Mini PCIe (Not assembled)
- USB
 - USB3.0 OTG Type C
 - USB3.0 Host Type A x 2
- AUDIO
 - 3.5mm Headphones jack
 - 3.5mm Line in jack
 - Digital Microphone
- µSD-Card slot
- Camera
 - Serial interface – Dual MIPI CSI x4 lanes each.
- NAND Flash (Not assembled)
- Debug
 - USB debug (UART1) - Type Micro AB
 - JTAG – Header
- RTC
 - ISL12057 Chip
- Additional
 - SAI (Serial Audio Interface) - Headers
 - UART, ECSPI, I2C, GPIO's - Headers
 - General purpose LED, Buttons (General Purpose + control)
- Power
 - 5V DC Input. - 2.0mm DC jack / 2 pin Terminal Block
 - 5V DC Out – 2 pin Header
 - RTC Backup battery - CR1225 Battery Holder

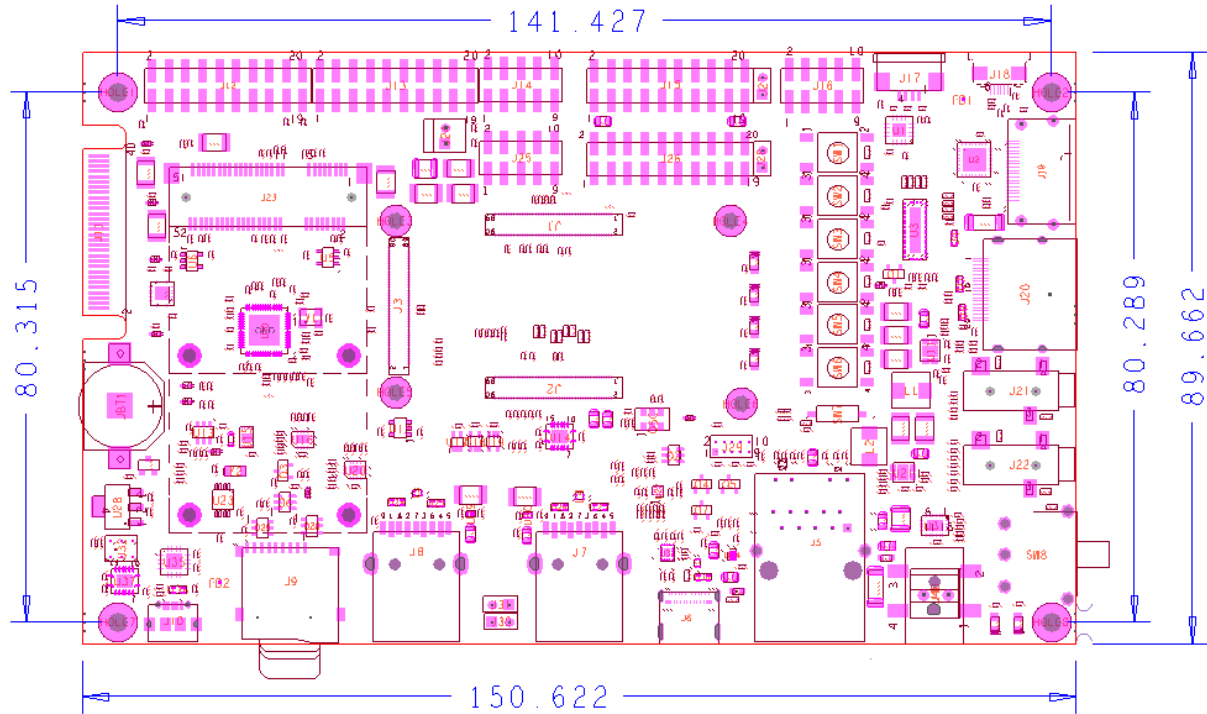
1.3 Block Diagram



VAR-DT8MCUSTOMBOARD CARRIER BOARD

1.4 Board Layout

The VAR-DT8MCustomBoard's physical dimensions are 151 x 90 mm.



Detailed CAD files are available for download at www.variscite.com.

1.5 VAR-DT8MCustomBoard connectors

The below table lists all available connectors on the VAR-DT8MCustomBoard, Refer to chapter 2 for a more detailed description and Pin-out of each connector.

Table 1-1 VAR-DT8MCustomBoard connectors

| Reference | Function | Type |
|-----------|---------------------------------|--|
| J1 | DART-MX8M J1 | Board to board, 90 pos., 0.4mm |
| J2 | DART-MX8M J2 | Board to board, 90 pos., 0.4mm |
| J3 | DART-MX8M J3 | Board to board, 90 pos., 0.4mm |
| J4 | Power In | DC IN Jack 2.0 mm |
| J5 | 10/100/1000Mbps ETH1 Port | RJ-45 |
| J6 | USB 3.0/2.0 OTG | USB Type C |
| J7 | USB 3.0 Host | USB 3.0 Type A |
| J8 | USB 3.0 Host | USB 3.0 Type A |
| J9 | SD-MMC | uSD Connector |
| J10 | USB Debug | USB Type micro AB |
| J11 | MIPI-CSI (4 lanes x 2 Cameras) | Edge Connector mates to HSEC8-130-01-SM-DV-A |
| J12 | UART, I2C | Header SMT, 10x2, 2.54mm |
| J13 | SAI2, SAI5 | Header SMT, 10x2, 2.54mm |
| J14 | GPIO, SPDIF | Header SMT, 5x2, 2.54mm |
| J15 | LVDS#1 (Clock & Data pairs 0-2) | Header SMT, 10x2, 2.54mm |
| J16 | ECSPI, BT/WIFI Host wake | Header SMT, 5x2, 2.54mm |
| J17 | Resistive Touch I/F | FFC/FPC 4-pin |
| J18 | Capacitive Touch Panel I/F | FFC/FPC 6-pin |
| J19 | HDMI | HDMI Type A Rcpt. SMT, R/A |
| J20 | Display Port | Display Port Rcpt. SMT, R/A |
| J21 | Line In | Audio Jack 3.5 mm |
| J22 | Headphones | Audio Jack 3.5 mm |
| J23 | Mini PCIe Conn #1 | Mini PCIe Conn, 2x26 0.8mm |
| J24 | FAN 5V | Header TH, 2x1, 2.54mm |
| J25 | SAI1 | Header SMT, 5x2, 2.54mm |
| J26 | LVDS#2 (Clock & Data pairs 0-2) | Header SMT, 5x2, 2.54mm |
| J27 | LVDS#1 (Data pair 3) | Header TH, 2x1, 2.54mm |
| J28 | LVDS#2 (Data pair 3) | Header TH, 2x1, 2.54mm |
| J29 | JTAG | Header TH, 5x2, 1.27mm |
| J32 | Mini PCIe Conn #2 | Mini PCIe Conn, 2x26 0.8mm |
| J40 | Power In | 2 Pin Terminal Block |
| JBT1 | RTC Battery Holder | CR1225 Battery Holder |
| | QSPI, NAND | Test points Bottom |

2 Detailed Description

2.1 Overview

This chapter details the VAR-DT8MCustomBoard features and external interfaces, some of which are driven directly by the DART-MX8M.

Please refer to the DART-MX8M data sheet for more information.

Table 2-1 describes this chapter table header and acronyms used.

Table 2-1: Acronyms used on tables column header

| Column | | Meaning |
|--------------------|----|--|
| Pin# | x | Pin number on a connector |
| Type | | Pin type & direction |
| | I | INPUT |
| | O | OUTPUT |
| | DS | Differential Signal |
| | A | Analog |
| | P | Power |
| Signal | | VAR-DT8MCustomBoard schematic signal name |
| Description | | Short Pin functionality description |

2.2 VAR-DT8MCustomBoard Interfaces

2.2.1 DART-MX8M

VAR-DT8MCustomBoard features x3 90 pin mating connectors to connect with the DART-MX8M System-on-module.

Please refer to the DART-MX8M module data sheet for a complete signal description and pin-out on J1, J2 and J3 connectors.

2.3 Standard External Interfaces

2.3.1 USB HOST & OTG

The DART-MX8M features two USB3.0/2.0 ports. Custom board implements the following:

- First port connected to a USB3.0/2.0 Type C OTG connector
- Second port connected to a USB3 four port hub which connects as follows:
 - Two hub ports connect to USB3.0/2.0 Type A Host Connectors
 - Two hub ports connect to the USB2.0 interface of two mPCIe connectors.

2.3.1.1 USB3.0/2.0 Type-C OTG Connector Pin-out (J6)

Table 2-2 USB Type-C OTG Connector Pin-out (J6)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---|
| A1 | GND | P | Ground return |
| A2 | SS_TX1_P | DSO | SuperSpeed diff. pair #1, TX, positive |
| A3 | SS_TX1_N | DSO | SuperSpeed diff. pair #1, TX, negative |
| A4 | USB_SS3_VBUS | P | Bus power |
| A5 | USB_SS3_CC1 | IO | Configuration channel |
| A6 | USB_C_OTG_DP | DSIO | Non-SuperSpeed diff. pair, pos. 1, positive |
| A7 | USB_C_OTG_DN | DSIO | Non-SuperSpeed diff. pair, pos. 1, negative |
| A8 | SBU1 | IO | Sideband use (SBU) |
| A9 | USB_SS3_VBUS | P | Bus power |
| A10 | SS_RX2_N | DSI | SuperSpeed diff. pair #4, RX, negative |
| A11 | SS_RX2_P | DSI | SuperSpeed diff. pair #4, RX, positive |
| A12 | GND | P | Digital Ground |
| B1 | GND | P | Digital Ground |
| B2 | SS_TX2_P | DSO | SuperSpeed diff. pair #3, TX, positive |
| B3 | SS_TX2_N | DSO | SuperSpeed diff. pair #3, TX, negative |
| B4 | USB_SS3_VBUS | P | Bus power |
| B5 | USB_SS3_CC2 | IO | Configuration channel |
| B6 | USB_C_OTG_DP | DSIO | Non-SuperSpeed diff. pair, pos. 2, positive |
| B7 | USB_C_OTG_DN | DSIO | Non-SuperSpeed diff. pair, pos. 2, negative |
| B8 | SBU2 | IO | Sideband use (SBU) |
| B9 | USB_SS3_VBUS | P | Bus power |
| B10 | SS_RX1_N | DSI | SuperSpeed diff. pair #2, RX, negative |
| B11 | SS_RX1_P | DSI | SuperSpeed diff. pair #2, RX, positive |
| B12 | GND | P | Digital Ground |
| SH1 | GND | P | SHIELD pin reference |
| SH2 | GND | P | SHIELD pin reference |
| SH3 | GND | P | SHIELD pin reference |
| SH4 | GND | P | SHIELD pin reference |

2.3.1.2 USB3.0/2.0 HOST Connector Pin-out (J7)

Table 2-3 USB3.0/2.0 Host Connector Pin-out (J7)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-------------------------------------|
| 1 | USB3_PRT2_PWR | P | Bus power |
| 2 | USB2_P2_C_DN | DSIO | Non-SuperSpeed diff. pair, negative |
| 3 | USB2_P2_C_DP | DSIO | Non-SuperSpeed diff. pair, positive |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|------------------------------------|
| 4 | GND | P | Digital Ground |
| 5 | USB2_P2_RXN | DSI | SuperSpeed diff. pair RX, negative |
| 6 | USB2_P2_RXP | DSI | SuperSpeed diff. pair RX, positive |
| 7 | GND | P | Digital Ground |
| 8 | USB2_P2_C_TXN | DSO | SuperSpeed diff. pair TX, negative |
| 9 | USB2_P2_C_TXP | DSO | SuperSpeed diff. pair TX, positive |
| 10 | GND | P | SHIELD pin reference |
| 11 | GND | P | SHIELD pin reference |

2.3.1.3 USB3.0/2.0 HOST Connector Pin-out (J8)

Table 2-4 USB3.0/2.0 Host Connector Pin-out (J8)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-------------------------------------|
| 1 | USB3_PRT1_PWR | P | Bus power |
| 2 | USB2_P1_C_DN | DSIO | Non-SuperSpeed diff. pair, negative |
| 3 | USB2_P1_C_DP | DSIO | Non-SuperSpeed diff. pair, positive |
| 4 | GND | P | Digital Ground |
| 5 | USB2_P1_RXN | DSI | SuperSpeed diff. pair RX, negative |
| 6 | USB2_P1_RXP | DSI | SuperSpeed diff. pair RX, positive |
| 7 | GND | P | Digital Ground |
| 8 | USB2_P1_C_TXN | DSO | SuperSpeed diff. pair TX, negative |
| 9 | USB2_P1_C_TXP | DSO | SuperSpeed diff. pair TX, positive |
| 10 | GND | P | SHIELD pin reference |
| 11 | GND | P | SHIELD pin reference |

2.3.2 uSD Card

uSD Card interface is driven by the SD/MMC2 interface of the of the DART-MX8M.

2.3.2.1 uSD card slot Connector Pin-out (J17)

Table 2-5 uSD Card Slot Connector Pin-out (J17)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 1 | CONN_SD2_DATA2 | IO | MMC Parallel Data2 |
| 2 | CONN_SD2_DATA3 | IO | MMC Parallel Data3 |
| 3 | CONN_SD2_CMD | IO | MMC Command |
| 4 | SW_3P3_SD2 | P | 3.3V supply from SOM; Supply is switchable |
| 5 | CONN_SD2_CLK_R | I | MMC Clock |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|----------------------|
| 6 | GND | P | Digital Ground |
| 7 | CONN_SD2_DATA0 | IO | MMC Parallel Data0 |
| 8 | CONN_SD2_DATA1 | IO | MMC Parallel Data1 |
| 9 | CONN_SD2_CD_B | O | MMC Card Detect |
| 10 | GND | P | SHIELD pin reference |
| 11 | GND | P | SHIELD pin reference |
| 12 | GND | P | SHIELD pin reference |
| 13 | GND | P | SHIELD pin reference |

2.3.3 Mini PCIe

The DART-MX8M PCI Express interface is exposed by the VAR-DT8MCustomBoard through a standard Mini PCI Express connector supporting connection of mini PCI Express expansion cards.

Two ports are available; PCIe port 1 connected to J23 and port 2 connected to J32.

2.3.3.1 Mini PCIe Connector Pin-out (J23)

Table 2-6 mini PCI Express Connector Pin-out (J23)

| Pin # | CustomBoard Signal | Type | Description |
|-------|-----------------------|------|--|
| 1 | | | |
| 2 | BASE_PER_3V3 | P | Base board 3.3V |
| 3 | | | |
| 4 | GND | P | Digital Ground |
| 5 | | | |
| 6 | BASE_PER_1V5#1 | P | Base board 1.5V #1 Limited to 300mA |
| 7 | | | |
| 8 | | | |
| 9 | GND | P | Digital Ground |
| 10 | | | |
| 11 | PCIE1_REFCLK100M_N | DSI | PCIe Clock Diff. Negative; 100MHz HCSL |
| 12 | | | |
| 13 | PCIE1_REFCLK100M_P | DSI | PCIe Clock Diff. Positive; 100MHz HCSL |
| 14 | | | |
| 15 | GND | P | Digital Ground |
| 16 | | | |
| 17 | | | |
| 18 | GND | P | Digital Ground |
| 19 | | | |
| 20 | | | |
| 21 | GND | P | Digital Ground |
| 22 | SAI1_RXD5(GPIO4_IO07) | O | PCIe Reset signal; GPIO4_IO07 <i>Note: Used by SOM for boot config @ power up</i> |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 23 | PCIE1_CRXM | DSI | PCIe Receive Lane Diff. Negative; SOC port #1 |
| 24 | BASE_PER_3V3 | P | Base board 3.3V |
| 25 | PCIE1_CRXP | DSI | PCIe Receive Lane Diff. Positive; SOC port #1 |
| 26 | GND | P | Digital Ground |
| 27 | GND | P | Digital Ground |
| 28 | BASE_PER_1V5#1 | P | Base board 1.5V #1 Limited to 300mA |
| 29 | GND | P | Digital Ground |
| 30 | I2C4_SCL | O | I2C #4 Clock |
| 31 | PCIE1_CTXM | DSO | PCIe Transmit Lane Diff. Negative; SOC port #1 |
| 32 | I2C4_SDA | IO | I2C #4 Data |
| 33 | PCIE1_CTXP | DSO | PCIe Transmit Lane Diff. Positive; SOC port #1 |
| 34 | GND | P | Digital Ground |
| 35 | GND | P | Digital Ground |
| 36 | USB_MPCIE1_DM | DSIO | USB2.0 Diff. Negative; USB Hub port #3 |
| 37 | GND | P | Digital Ground |
| 38 | USB_MPCIE1_DP | DSIO | USB2.0 Diff. Positive; USB Hub port #3 |
| 39 | BASE_PER_3V3 | P | Base board 3.3V |
| 40 | GND | P | Digital Ground |
| 41 | BASE_PER_3V3 | P | Base board 3.3V |
| 42 | | | |
| 43 | GND | P | Digital Ground |
| 44 | | | |
| 45 | | | |
| 46 | | | |
| 47 | | | |
| 48 | BASE_PER_1V5#1 | P | Base board 1.5V #1 Limited to 300mA |
| 49 | | | |
| 50 | GND | P | Digital Ground |
| 51 | | | |
| 52 | BASE_PER_3V3 | P | Base board 3.3V |

2.3.3.2 Mini PCIe Connector Pin-out (J32)

Table 2-7 mini PCI Express Connector Pin-out (J32)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-----------------|
| 1 | | | |
| 2 | BASE_PER_3V3 | P | Base board 3.3V |

VAR-DT8MCUSTOMBOARD CARRIER BOARD

| Pin # | CustomBoard Signal | Type | Description |
|-------|-----------------------|------|--|
| 3 | | | |
| 4 | GND | P | Digital Ground |
| 5 | | | |
| 6 | BASE_PER_1V5#2 | P | Base board 1.5V #2 Limited to 300mA |
| 7 | | | |
| 8 | | | |
| 9 | GND | P | Digital Ground |
| 10 | | | |
| 11 | PCIE2_REFCLK100M_N | DSI | PCIe Clock Diff. Negative; 100MHz HCSL |
| 12 | | | |
| 13 | PCIE2_REFCLK100M_P | DSI | PCIe Clock Diff. Positive; 100MHz HCSL |
| 14 | | | |
| 15 | GND | P | Digital Ground |
| 16 | | | |
| 17 | | | |
| 18 | GND | P | Digital Ground |
| 19 | | | |
| 20 | | | |
| 21 | GND | P | Digital Ground |
| 22 | SAI1_TXD7(GPIO4_IO19) | O | PCIe Reset signal; GPIO4_IO19 <i>Note: Used by SOM for boot config @ power up</i> |
| 23 | PCIE2_CRXM | DSI | PCIe Receive lane Diff. Negative; SOC port #2 |
| 24 | BASE_PER_3V3 | P | Base board 3.3V |
| 25 | PCIE2_CRXP | DSI | PCIe Receive lane Diff. Positive; SOC port #2 |
| 26 | GND | P | Digital Ground |
| 27 | GND | P | Digital Ground |
| 28 | BASE_PER_1V5#2 | P | Base board 1.5V #2 Limited to 300mA |
| 29 | GND | P | Digital Ground |
| 30 | I2C4_SCL | O | I2C #4 Clock |
| 31 | PCIE2_CTXM | DSO | PCIe Transmit lane Diff. Negative; SOC port #2 |
| 32 | I2C4_SDA | IO | I2C #4 Data |
| 33 | PCIE2_CTXP | DSO | PCIe Transmit lane Diff. Positive; SOC port #2 |
| 34 | GND | P | Digital Ground |
| 35 | GND | P | Digital Ground |
| 36 | USB_MPCIE2_DM | DSIO | USB2.0 Diff. Negative; USB Hub port #4 |
| 37 | GND | P | Digital Ground |
| 38 | USB_MPCIE2_DP | DSIO | USB2.0 Diff. Positive; USB Hub port #4 |
| 39 | BASE_PER_3V3 | P | Base board 3.3V |
| 40 | GND | P | Digital Ground |

VAR-DT8MCUSTOMBOARD CARRIER BOARD

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-------------------------------------|
| 41 | BASE_PER_3V3 | P | Base board 3.3V |
| 42 | | | |
| 43 | GND | P | Digital Ground |
| 44 | | | |
| 45 | | | |
| 46 | | | |
| 47 | | | |
| 48 | BASE_PER_1V5#2 | P | Base board 1.5V #2 Limited to 300mA |
| 49 | | | |
| 50 | GND | P | Digital Ground |
| 51 | | | |
| 52 | BASE_PER_3V3 | P | Base board 3.3V |

Note

1. J32 located on the print side and is not assembled.
 2. To enable the PCIe reference clock for J32, R120 should be removed.
 3. Enabling the interface in the DTS file, with no reference clock running will prevent full boot.
-

2.3.4 Ethernet

The VAR-DT8MCustomBoard connects the DART-MX8M Gigabit Ethernet interface, sourced by its' PHY, to a standard RJ45 Ethernet jack connector with integrated magnetics. Please refer to the DART-MX8M datasheet for more information.

2.3.4.1 10/100/1000BaseT RJ45 Connector Pin-out (J5)

Table 2-8 10/100/1000BaseT RJ45 Connector Pin-out (J5)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--------------------------------------|
| R1 | ETH_TRX0_P | DSIO | Bi-directional diff. pair A positive |
| R2 | ETH_TRX0_N | DSIO | Bi-directional diff. pair A negative |
| R3 | ETH_TRX1_P | DSIO | Bi-directional diff. pair B positive |
| R4 | ETH_TRX1_N | DSIO | Bi-directional diff. pair B negative |
| R5 | ETH_TRCT1 | O | Primary transformer common pin |
| R6 | ETH_TRCT2 | O | Primary transformer common pin |
| R7 | ETH_TRX2_P | DSIO | Bi-directional diff. pair C positive |
| R8 | ETH_TRX2_N | DSIO | Bi-directional diff. pair C negative |
| R9 | ETH_TRX3_P | DSIO | Bi-directional diff. pair D positive |
| R10 | ETH_TRX3_N | DSIO | Bi-directional diff. pair D negative |
| L1 | GND | P | Digital Ground |
| L2 | LED_ACT | O | Activity LED Anode; |
| L3 | LED_LINK10_100 | IO | Link 10/100 LED Anode; |
| | | | Link 1000 LED Cathode; |
| L4 | LED_LINK1000 | IO | Link 1000 LED Anode; |
| | | | Link 10/100 LED Cathode; |
| SH1 | GND_EARTH | P | EARTH |
| SH2 | GND_EARTH | P | EARTH |

Note

For detailed LED behavior see LED status table in SOM data sheet.

2.3.5 AUDIO

The VAR-DT8MCustomBoard features two 3.5mm jacks for analog audio interfaces.

- Headphone
- Line in

The analog audio interface signals are driven by the DART-MX8M CODEC. Please refer to the DART-MX8M data sheet for complete audio codec information.

Also, a digital microphone is implemented on the VAR-DT8MCustomBoard, see schematics for U32.

2.3.5.1 Line In Jack Connector Pin-out (J21)

Table 2-9 Line in Jack Connector Pin-out (J21)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------------|
| 1 | AGND | AP | Analog ground return for audio. |
| 2 | LLINEIN_C | AI | Line in Left input |
| 3 | RLINEIN_C | AI | Line in Left input |

2.3.5.2 Headphone jack Connector Pin-out (J22)

Table 2-10 Headphone out Jack Connector Pin-out (J22)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------------|
| 1 | AGND | AP | Analog ground return for audio. |
| 2 | HPLOUT_C | AO | Headphone out Left |
| 3 | HPROUT_C | AO | Headphone out Right |

2.3.6 Serial Camera

The VAR-DT8MCustomBoard supports two MIPI CSI camera sensor inputs using an extension camera board connected to an edge connector in the VAR-DT8CustomBoard.

The Camera Board Mating connector: SAMTEC 60POS 0.8mm pitch, **HSEC8-130-01-SM-DV-A**

2.3.6.1 Serial Camera Connector Pin-out (J11)

Table 2-11 Serial Camera Connector Pin-out (J11)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-----------------|
| 1 | BASE_PER_3V3 | P | Base board 3.3V |
| 2 | GND | P | Digital Ground |
| 3 | BASE_PER_3V3 | P | Base board 3.3V |
| 4 | I2C4_SDA_1V8 | IO | I2C #4 Data |

VAR-DT8MCUSTOMBOARD CARRIER BOARD

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 5 | BASE_PER_1V8 | P | Base board 1.8V |
| 6 | I2C4_SCL_1V8 | IO | I2C #4 Clock |
| 7 | BASE_PER_1V8 | P | Base board 1.8V |
| 8 | GND | P | Digital Ground |
| 9 | GND | P | Digital Ground |
| 10 | CSI_P2_PWRDN_1V8 | O | Power down control; Active Low; GPIO4_IO9 <i>Note: Used by SOM for boot config @ power up</i> |
| 11 | CSI_P1_DP0 | DSI | CSI Port1 Lane0; Positive |
| 12 | CSI_P2_RSTN_1V8 | O | Reset control; Active Low; GPIO5_IO29 <i>Note: Used by SOM for boot config @ power up</i> |
| 13 | CSI_P1_DN0 | DSI | CSI Port1 Lane0; Negative |
| 14 | | | |
| 15 | GND | P | Digital Ground |
| 16 | | | |
| 17 | CSI_P1_CKP | DSI | CSI Port1 Clock; Positive |
| 18 | GND | P | Digital Ground |
| 19 | CSI_P1_CKN | DSI | CSI Port1 Clock; Negative |
| 20 | | | |
| 21 | GND | P | Digital Ground |
| 22 | GND | P | Digital Ground |
| 23 | CSI_P1_DP1 | DSI | CSI Port1 Lane1; Positive |
| 24 | CSI_P2_DN3 | DSI | CSI Port2 Lane3; Negative |
| 25 | CSI_P1_DN1 | DSI | CSI Port1 Lane1; Negative |
| 26 | CSI_P2_DP3 | DSI | CSI Port2 Lane3; Positive |
| 27 | GND | P | Digital Ground |
| 28 | GND | P | Digital Ground |
| 29 | CSI_P1_DP2 | DSI | CSI Port1 Lane2; Positive |
| 30 | CSI_P2_DN2 | DSI | CSI Port2 Lane2; Negative |
| 31 | CSI_P1_DN2 | DSI | CSI Port1 Lane2; Negative |
| 32 | CSI_P2_DP2 | DSI | CSI Port2 Lane2; Positive |
| 33 | GND | P | Digital Ground |
| 34 | GND | P | Digital Ground |
| 35 | CSI_P1_DP3 | DSI | CSI Port1 Lane3; Positive |
| 36 | CSI_P2_DN1 | DSI | CSI Port2 Lane1; Negative |
| 37 | CSI_P1_DN3 | DSI | CSI Port1 Lane3; Negative |
| 38 | CSI_P2_DP1 | DSI | CSI Port2 Lane1; Positive |
| 39 | GND | P | Digital Ground |
| 40 | GND | P | Digital Ground |
| 41 | | | |
| 42 | CSI_P2_CKN | DSI | CSI Port2 Clock; Negative |
| 43 | GND | P | Digital Ground |
| 44 | CSI_P2_CKP | DSI | CSI Port2 Clock; Positive |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---|
| 45 | | | |
| 46 | GND | P | Digital Ground |
| 47 | | | |
| 48 | CSI_P2_DN0 | DSI | CSI Port2 Lane0; Negative |
| 49 | CSI_P1_RSTN_1V8 | O | Reset control; Active Low; GPIO5_IO28 |
| 50 | CSI_P2_DP0 | DSI | CSI Port2 Lane0; Positive |
| 51 | CSI_P1_PWRDN_1V8 | O | Power down control; Active High; GPIO4_IO08 |
| 52 | GND | P | Digital Ground |
| 53 | GND | P | Digital Ground |
| 54 | BASE_PER_1V8 | P | Base board 1.8V |
| 55 | I2C2_SCL_1V8 | IO | I2C #2 Clock |
| 56 | BASE_PER_1V8 | P | Base board 1.8V |
| 57 | I2C2_SDA_1V8 | IO | I2C #2 Data |
| 58 | BASE_PER_3V3 | P | Base board 3.3V |
| 59 | GND | P | Digital Ground |
| 60 | BASE_PER_3V3 | P | Base board 3.3V |

Note

Camera control (reset, power down) and I2C interfaces runs at 1.8V levels.

2.3.7 LVDS & DSI Display

The VAR-DT8MCustomBoard exposes the Dual-Link LVDS interface the MIPI-DSI to FlatLink™ bridge assembled on the DART-MX8M.

The interface is exposed to two Variscite standard 20 pin Headers; Fourth data bit of each interface is extended using additional 2 pin connector.

J26 and J28, FlatLink™ Channel 2 connectors will carry the MIPI-DSI Lanes when the SOM configuration is without "LD" configuration.

J15 used for connecting Variscite's standard 7" LVDS LCD screen.

Refer to the DART-MX8M data sheet for detailed description of the FlatLink™ interface.

2.3.7.1 LVDS#1 Connector Pin-out (J15)

Table 2-12 LVDS Channel 1 Connector Pin-out (J15)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------|
| 1 | BASE_PER_3V3 | P | Base power 3.3V |
| 2 | BASE_PER_3V3 | P | Base power 3.3V |
| 3 | GND | P | Digital Ground |
| 4 | GND | P | Digital Ground |
| 5 | LVDS1_TX0_N | DSO | LVDS Data0 Diff. Negative |

| Pin # | CustomBoard Signal | Type | Description |
|-------|----------------------|------|---|
| 6 | LVDS1_TX0_P | DSO | LVDS Data0 Diff. Positive |
| 7 | GND | P | Digital Ground |
| 8 | LVDS1_TX1_N | DSO | LVDS Data1 Diff. Negative |
| 9 | LVDS1_TX1_P | DSO | LVDS Data1 Diff. Positive |
| 10 | GND | P | Digital Ground |
| 11 | LVDS1_TX2_N | DSO | LVDS Data2 Diff. Negative |
| 12 | LVDS1_TX2_P | DSO | LVDS Data2 Diff. Positive |
| 13 | GND | P | Digital Ground |
| 14 | LVDS1_CLK_N | DSO | LVDS Clock Diff. Negative |
| 15 | LVDS1_CLK_P | DSO | LVDS Clock Diff. Positive |
| 16 | GND | P | Digital Ground |
| 17 | VCC_5V | P | Backlight LED 5V power |
| 18 | VCC_5V | P | Backlight LED 5V power |
| 19 | GPIO1_IO01(PWM1_OUT) | IO | Backlight Brightness Control; GPIO1_IO01 |
| 20 | GND | P | Digital Ground |

2.3.7.2 LVDS#1 Data3 Extension Connector Pin-out (J27)

Table 2-13 LVDS Channel 1 Data3 Connector Pin-out (J27)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------|
| 1 | LVDS1_TX3_N | DSO | LVDS Data3 Diff. Negative |
| 2 | LVDS1_TX3_P | DSO | LVDS Data3 Diff. Positive |

2.3.7.3 LVDS#2 Connector Pin-out (J26)

Table 2-14 LVDS Channel 2 Connector Pin-out (J26)

| Pin # | CustomBoard Signal | Type | Description |
|-------|---------------------|------|---------------------------|
| 1 | BASE_PER_3V3 | P | Base power 3.3V |
| 2 | BASE_PER_3V3 | P | Base power 3.3V |
| 3 | GND | P | Digital Ground |
| 4 | GND | P | Digital Ground |
| 5 | LVDS2_DSI_TX0_N | DSO | LVDS Data0 Diff. Negative |
| 6 | LVDS2_DSI_TX0_P | DSO | LVDS Data0 Diff. Positive |
| 7 | GND | P | Digital Ground |
| 8 | LVDS2_DSI_TX1_N | DSO | LVDS Data1 Diff. Negative |
| 9 | LVDS2_DSI_TX1_P | DSO | LVDS Data1 Diff. Positive |
| 10 | GND | P | Digital Ground |
| 11 | LVDS2_TX2_DSI_CLK_N | DSO | LVDS Data2 Diff. Negative |
| 12 | LVDS2_TX2_DSI_CLK_P | DSO | LVDS Data2 Diff. Positive |
| 13 | GND | P | Digital Ground |
| 14 | LVDS2_CLK_DSI_TX2_N | DSO | LVDS Clock Diff. Negative |

| Pin # | CustomBoard Signal | Type | Description |
|-------|----------------------|------|---|
| 15 | LVDS2_CLK_DSI_TX2_P | DSO | LVDS Clock Diff. Positive |
| 16 | GND | P | Digital Ground |
| 17 | VCC_5V | P | Backlight LED 5V power |
| 18 | VCC_5V | P | Backlight LED 5V power |
| 19 | GPIO1_IO01(PWM1_OUT) | IO | Backlight Brightness Control; GPIO1_IO01 |
| 20 | GND | P | Digital Ground |

Note

1. Connector carries the native MIPI-DSI lanes of the DART-MX8M SOC when configuration is without "LD"
 2. LVDS Data2 become MIPI-DSI CLK
 3. LVDS CLK become MIPI-DSI Lane2
-

2.3.7.4 LVDS#2 Data3 Extension Connector Pin-out (J28)

Table 2-15 LVDS Channel 2 Data3 Connector Pin-out (J28)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------|
| 1 | LVDS2_DSI_TX3_P | DSO | LVDS Data3 Diff. Positive |
| 2 | LVDS2_DSI_TX3_N | DSO | LVDS Data3 Diff. Negative |

Note

See J26 table note for DSI function

2.3.8 HDMI & DP Display

The VAR-DT8MCustomBoard exposes the shared pin function of the DART-MX8M for the HDMI and Display Port interfaces.

On the custom board it is implemented using a multiplexer routing the signals either to the HDMI or DP connector. Switch between the two implemented via different DTS files.

The interface is exposed to a standard HDMI and DP connectors.

**DISCLAIMER: DP/eDP INTERFACE NOT VALIDATED.
AWAITS NXP FORMAL RELEASE.**

Refer to the DART-MX8M data sheet for detailed description of these interfaces and HDMI termination.

2.3.8.1 HDMI Connector Pin-out (J19)

Table 2-16 HDMI Connector Pin-out (J19)

| Pin # | CustomBoard Signal | Type | Description |
|-------|-----------------------|------|---|
| 1 | HDMI_CON_D2_P | DSO | HDMI TMDS Diff. Data 2; Positive |
| 2 | GND | P | Digital Ground |
| 3 | HDMI_CON_D2_N | DSO | HDMI TMDS Diff. Data 2; Negative |
| 4 | HDMI_CON_D1_P | DSO | HDMI TMDS Diff. Data 1; Positive |
| 5 | GND | P | Digital Ground |
| 6 | HDMI_CON_D1_N | DSO | HDMI TMDS Diff. Data 1; Negative |
| 7 | HDMI_CON_D0_P | DSO | HDMI TMDS Diff. Data 0; Positive |
| 8 | GND | P | Digital Ground |
| 9 | HDMI_CON_D0_N | DSO | HDMI TMDS Diff. Data 0; Negative |
| 10 | HDMI_CON_CK_P | DSO | HDMI TMDS Diff. Clock; Positive |
| 11 | GND | P | Digital Ground |
| 12 | HDMI_CON_CK_N | DSO | HDMI TMDS Diff. Clock; Negative |
| 13 | HDMI_CEC_CON | IO | Consumer Electronics Control; 1 Wire Serial; Bidirectional |
| 14 | HDMI_UTILITY/HEAC+_CN | DSIO | HDMI_UTILITY signal; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Positive |
| 15 | HDMI_SCL_CON | O | I2C Serial Clock for DDC (Data Display Channel) |
| 16 | HDMI_SDA_CON | IO | I2C Serial Data for DDC (Data Display Channel) |
| 17 | GND | P | Digital Ground |
| 18 | HDMI_5V_CON | P | HDMI 5V Power out |
| 19 | HDMI_HPD/HEAC-_CN | DSIO | HDMI Hot Plug Detect; Alternatively, can be HDMI Ethernet and Audio Return Channel Diff. Negative |
| MTG1 | HDMI_EDP_SHLD | P | SHIELD pin reference |
| MTG2 | HDMI_EDP_SHLD | P | SHIELD pin reference |
| MTG3 | HDMI_EDP_SHLD | P | SHIELD pin reference |
| MTG4 | HDMI_EDP_SHLD | P | SHIELD pin reference |

2.3.8.2 DisplayPort Connector Pin-out (J20)

Table 2-17 DisplayPort Connector Pin-out (J20)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|-----------------------------------|
| 1 | HDMI_D0_B_P | DSO | Display Port Lane0 Diff. Positive |
| 2 | GND | P | Digital Ground |
| 3 | HDMI_D0_B_N | DSO | Display Port Lane0 Diff. Negative |
| 4 | HDMI_D1_B_P | DSO | Display Port Lane1 Diff. Positive |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 5 | GND | P | Digital Ground |
| 6 | HDMI_D1_B_N | DSO | Display Port Lane1 Diff. Negative |
| 7 | HDMI_D2_B_P | DSO | Display Port Lane2 Diff. Positive |
| 8 | GND | P | Digital Ground |
| 9 | HDMI_D2_B_N | DSO | Display Port Lane2 Diff. Negative |
| 10 | HDMI_D3_B_P | DSO | Display Port Lane3 Diff. Positive |
| 11 | GND | P | Digital Ground |
| 12 | HDMI_D3_B_N | DSO | Display Port Lane3 Diff. Negative |
| 13 | DP_CFG1 | P | Connected to ground (Other function when used for DVI/HDMI mode) |
| 14 | DP_CFG2 | P | Connected to ground (Other function when used for DVI/HDMI mode) |
| 15 | HDMI_AUX_B_C_P | DSO | Auxiliary channel Diff. Positive |
| 16 | GND | P | Digital Ground |
| 17 | HDMI_AUX_B_C_N | DSO | Auxiliary channel Diff. Negative |
| 18 | HDMI_HPD_B | I | Hot Plug Detect signal |
| 19 | GND | P | Digital Ground |
| 20 | BASE_PER_3V3 | P | Base board 3.3V |
| MECH1 | HDMI_EDP_SHLD | P | SHIELD pin reference |
| MECH2 | HDMI_EDP_SHLD | P | SHIELD pin reference |

2.3.9 Capacitive Touch

The DART-MX8M provides a capacitive Touch interface exposed to a FFC/FPC connector for connecting to Variscite's standard 7" Capacitive touch LCD screen.

2.3.9.1 Capacitive Touch Panel Connector Pin-out (J18)

Table 2-18 Capacitive Touch Panel Connector Pin-out (J18)

| Pin # | CustomBoard Signal | Type | Description |
|-------|-----------------------|------|---|
| 1 | SAI1_RXD3(GPIO4_IO05) | IO | Capacitive Touch Reset; Active Low; GPIO4_IO05 <i>Note: Used by SOM for boot config @ power up</i> |
| 2 | I2C2_SDA | IO | I2C #2 Clock |
| 3 | I2C2_SCL | IO | I2C #2 Data |
| 4 | GPIO1_IO14 | IO | Capacitive Touch Interrupt; Active Low; GPIO1_IO14 |
| 5 | BASE_PER_3V3 | P | Base board 3.3V |
| 6 | GND | P | Digital Ground |
| 7 | GND | P | Digital Ground |
| 8 | GND | P | Digital Ground |

2.3.10 Resistive Touch

The VAR-DT8MCustomBoard provides a resistive interface exposed to a FFC/FPC connector for connecting to resistive touch LCD screen.

2.3.10.1 Resistive Touch Connector Pin-out (J17)

Table 2-19 Resistive Touch Connector Pin-out (J17)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|----------------------------------|
| 1 | TS_X- | AI | X negative side plate connection |
| 2 | TS_Y+ | AI | Y positive side plate connection |
| 3 | TS_X+ | AI | X positive side plate connection |
| 4 | TS_Y- | AI | Y negative side plate connection |
| 5 | GND | P | Digital Ground |
| 6 | GND | P | Digital Ground |

2.3.11 USB - Debug

The DART-MX8M exposes the debug UART1 interface to the VAR-DT8MCustomBoard. The signals are driven by an on-board UART-to-USB Bridge and exposed to a Micro USB connector.

2.3.11.1 USB Debug Connector Pin-out (J10)

Table 2-20 USB Debug Connector Pin-out (J10)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--------------------------------------|
| 1 | DEBUG_VBUS_C | P | 5V power input |
| 2 | USB_DEBUG_DM | DSIO | USB Data Negative |
| 3 | USB_DEBUG_DP | DSIO | USB Data Positive |
| 4 | GND | I | USB Micro ID signal (Slave function) |
| 5 | GND | P | Digital Ground |
| 6 | GND | P | SHIELD pin reference |
| 7 | GND | P | SHIELD pin reference |
| 10 | GND | P | SHIELD pin reference |
| 11 | GND | P | SHIELD pin reference |

2.3.12 I2C & UART & ENET MDIO

The VAR-DT8MCustomBoard exposes DART-MX8M I2C, UART and ENET MDIO interfaces. Both are exported to a standard 20 pin Header.

UART4 is used on SOMs with "WBD" configuration. See DART-MX8M data sheet for details on using externally with this configuration.

UART2 on the header implements FTDI adapter connector layout for simple conversion to USB by external module.

2.3.12.1 I2C and UART Connector Pin- out (J12)

Table 2-21 I2C, UART and ENET MDIO Connector Pin-out (J12)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---|
| 1 | BT_UART4_TX | IO | UART4 Transmit <i>Note: Used by SOM in "WBD" configuration</i> |
| 2 | FTDI_RTSN | O | FTDI Header Ready To Send; Active Low |
| 3 | BT_UART4_CTS_B | IO | UART4 Clear To Send <i>Note: Used by SOM in "WBD" configuration</i> |
| 4 | FTDI_RXI | IO | UART2 Transmit |
| 5 | BT_UART4_RX | IO | UART4 Receive <i>Note: Used by SOM in "WBD" configuration</i> |
| 6 | FTDI_TXO | IO | UART2 Receive |
| 7 | BT_UART4_RTS_B | IO | UART4 Ready To Send <i>Note: Used by SOM in "WBD" configuration</i> |
| 8 | | | |
| 9 | BASE_PER_3V3 | P | Base board 3.3V; |
| 10 | FTDI_CTSN | I | FTDI Header Clear To Send; Active Low |
| 11 | UART3_RXD | IO | UART3 Receive |
| 12 | GND | P | Digital Ground |
| 13 | UART3_TXD | | UART3 Transmit |
| 14 | ENET_MDIO | IO | ENET Management Data; <i>Note: Shared with SOM in "EC" Configuration Run at 2.5V levels in this configuration</i> |
| 15 | GND | P | Digital Ground |
| 16 | ENET_MDC | O | ENET Management Clock; <i>Note: Shared with SOM in "EC" Configuration Run at 2.5V levels in this configuration</i> |
| 17 | I2C4_SCL | IO | I2C #4 Clock |
| 18 | I2C3_SCL | IO | I2C #3 Clock <i>Note: Shared by SOM all configurations; 10K Pullup included on SOM</i> |
| 19 | I2C4_SDA | IO | I2C #4 Data |
| 20 | I2C3_SDA | IO | I2C #3 Data <i>Note: Shared by SOM all configurations; 10K pullup included on SOM</i> |

2.3.13 GPIO & Digital Audio(SPDIF)

The VAR-DT8MCustomBoard exports the DART-MX8M optional GPIO's and SPDIF through a standard 10 pin Header.

2.3.13.1 GPIO & SPDIF Pin-out (J14)

Table 2-22 GPIOs and SPDIF Connector Pin-out (J14)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---|
| 1 | BASE_PER_3V3 | P | Base power 3.3V |
| 2 | GPIO1_IO11 | IO | GPIO1_IO11 <i>Note: Used by SOM in "LD" configuration</i> |
| 3 | SPDIF_RX | IO | SPDIF Receive Data |
| 4 | GPIO1_IO12 | IO | GPIO1_IO12 |
| 5 | SPDIF_EXT_CLK | IO | SPDIF External Clock <i>Note: Used by SOM in "WBD" configuration</i> |
| 6 | GPIO1_IO08 | IO | GPIO1_IO08 <i>Note: Used by SOM in "WBD" configuration</i> |
| 7 | SPDIF_TX | IO | SPDIF Transmit Data |
| 8 | GPIO1_IO15 | IO | GPIO1_IO15 <i>Note: Connected on custom board to RTC_IRQn Via a series resistor.</i> |
| 9 | GND | P | Digital Ground |
| 10 | GPIO1_IO06 | IO | GPIO1_IO06 |

2.3.14 Digital Audio (SAI1 & SAI2 & SAI5)

The VAR-DT8MCustomBoard exports the DART-MX8M SAI1, SAI2 and SAI5 signals through a standard 10 pin Headers.

See DART-MX8M data sheet for other configurations of SAI.

2.3.14.1 SAI2 & SAI5 Header Pin-out (J13)

Table 2-23 SAI2 & SAI5 Header Pin-out (J13)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 1 | BASE_PER_3V3 | P | Base board 3.3V |
| 2 | EN_SOM_VBAT_3V3 | I | SOM 3.3V regulator enable input |
| 3 | BASE_PER_1V8 | P | Base board 1.8V |
| 4 | GND | P | Digital Ground |
| 5 | SAI2_RXC | IO | SAI2 Receive Bit Clock |
| 6 | PMIC_STBY_REQ | IO | SOM PMIC standby request; If used isolate with high impedance input |
| 7 | SAI2_RXFS | IO | SAI2 Receive Frame Sync |
| 8 | SAI5_RXC | IO | SAI2 Receive Bit Clock |
| 9 | SAI2_RXD0 | IO | SAI2 Receive Data 0 |
| 10 | SAI5_RXFS | IO | SAI5 Receive Frame Sync |
| 11 | SAI2_TXC | IO | SAI2 Transmit Bit Clock |
| 12 | SAI5_RXD0 | IO | SAI5 Receive Data 0 |

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------------------|
| 13 | SAI2_TXFS | IO | SAI2 Transmit Frame Sync |
| 14 | SAI5_RXD1 | IO | SAI5 Receive Data 1 |
| 15 | SAI2_TXD0 | IO | SAI2 Transmit Data 0 |
| 16 | SAI5_RXD2 | IO | SAI5 Receive Data 2 |
| 17 | SAI2_MCLK | IO | SAI2 Master Clock |
| 18 | SAI5_RXD3 | IO | SAI2 Receive Data 0 |
| 19 | VCC_5V | P | Base board 5V; Protected for OV |
| 20 | SAI5_MCLK | IO | SAI5 Master Clock |

2.3.14.2 SAI1 Header Pin-out (J25)

Table 2-24 SAI1 Header Pin-out (J25)

| Pin # | CustomBoard Signal | Type | Description |
|-------|-----------------------|------|--|
| 1 | SAI1_TXD4(GPIO4_IO16) | IO | SAI1 Transmit Data 4 <i>Note: Used by SOM for boot config @ power up</i> |
| 2 | SAI1_RXFS | IO | SAI1 Receive Frame Sync |
| 3 | SAI1_TXD0(GPIO4_IO12) | IO | SAI1 Transmit Data 0 <i>Note: Used by SOM for boot config @ power up</i> |
| 4 | SAI1_RXC | IO | SAI1 Receive Bit Clock |
| 5 | SAI1_TXC(GPIO4_IO11) | IO | SAI1 Transmit Bit Clock |
| 6 | SAI1_RXD0(GPIO4_IO02) | IO | SAI1 Receive Data 0 <i>Note: Used by SOM for boot config @ power up</i> |
| 7 | SAI1_TXFS(GPIO4_IO10) | IO | SAI1 Transmit Frame Sync |
| 8 | SAI1_MCLK(GPIO4_IO20) | IO | SAI1 Master Clock |
| 9 | SOM_WIFI32K | IO | GPIO1_IO00 <i>Note: Used by SOM as 32.768Khz reference clock with "WBD" Configuration</i> |
| 10 | GND | P | Digital Ground |

NOTE

SAI1 TXD[7..0] and RXD[7..0] pins are used by DART-MX8M for boot config. Care should be given not to drive them before rise of POR_B signal + 1ms; See "Boot Configuration" in DART-MX8M data sheet.

2.3.15 ECSPi & BT/WIFI Host Wake

The VAR-DT8MCustomBoard exports the following DART-MX8M signals through a standard 10 pin Header:

1. ECSPi1 interface
2. BT and WIFI Host wake signals available from the DART-MX8M WIFI module (in case of "WBD" configuration only)
3. GPIO line to be connected to the host wake signal, running in the same levels.
4. POR_B

2.3.15.1 ECSP11 & BT/WIFI Host Wake Header Pin-out (J16)

Table 2-25 ECSP11 & BT/WIFI Host Wake Header Pin-out (J16)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 1 | BT_HOST_WAKE | O | SOM WIFI module Bluetooth host wake |
| 2 | ECSP11_SCLK | IO | SPI Serial Clock |
| 3 | SD2_WP(GPIO2_IO20) | IO | GPIO2_IO20; 1.8V/3.3V levels depends on SD2 interface |
| 4 | ECSP11_SS0 | IO | SPI Slave Select; Active Low |
| 5 | WIFI_HOST_WAKE | O | SOM WIFI module WIFI host wake |
| 6 | ECSP11_MOSI | IO | SPI Master Out Slave In |
| 7 | POR_B | IO | SOM Power On Reset; Active Low; Driven by SOM PMIC; Open Drain |
| 8 | ECSP11_MISO | IO | SPI Master In Slave Out |
| 9 | GND | P | Digital Ground |
| 10 | GND | P | Digital Ground |

Note

4. ECSP11 interface used for the resistive touch controller employed on the custom board. In order to use the interface via this header ECSP11_MISO need to be disconnected from the resistive controller OR use a different GPIO as slave select.
5. BT HOST wake and/or WIFI HOST wake signals can be connected to GPIO2_IO20 to use this function; Logic is required to use both.

2.3.16 QSPIA & QSPIB

The VAR-DT8MCustomBoard exports the following DART-MX8M QSPI and NAND signals through test points connected in parallel to a standard NAND device footprint. Both interfaces share the same pins on the SOM.

QSPIA and QSPIB test points and NAND device are located on the print side. For NAND and other functions of these pins refer to the DART-MX8M data sheet.

2.3.16.1 QSPIA & QSPIB Test points

Table 2-26 QSPI Test Points

| # | CustomBoard TP designator | Type | Description |
|---|---------------------------|------|---------------|
| 1 | GPIO3_IO16-TP1 | IO | GPIO3_IO16 |
| 2 | GPIO3_IO17-TP1 | IO | GPIO3_IO17 |
| 3 | GPIO3_IO18-TP1 | IO | GPIO3_IO18 |
| 4 | QSPIA_DATA0-TP1 | IO | QSPI A Data 0 |
| 5 | QSPIA_DATA1-TP1 | IO | QSPI A Data 1 |

| # | CustomBoard TP designator | Type | Description |
|----|---------------------------|------|-----------------------------------|
| 6 | QSPIA_DATA2-TP1 | IO | QSPI A Data 2 |
| 7 | QSPIA_DATA3-TP1 | IO | QSPI A Data 3 |
| 8 | QSPIA_DQS-TP1 | IO | QSPI A Strobe |
| 9 | QSPIA_SCLK-TP1 | IO | QSPI A Serial Clock |
| 10 | QSPIA_SS0_B-TP1 | IO | QSPI A Slave Select 0; Active Low |
| 11 | QSPIB_DATA0-TP1 | IO | QSPI B Data 0 |
| 12 | QSPIB_DATA1-TP1 | IO | QSPI B Data 1 |
| 13 | QSPIB_DATA2-TP1 | IO | QSPI B Data 2 |
| 14 | QSPIB_DATA3-TP1 | IO | QSPI B Data 3 |
| 15 | QSPIB_DQS-TP1 | IO | QSPI B Strobe |
| 16 | QSPIB_SCLK-TP1 | IO | QSPI B Serial Clock |
| 17 | QSPIB_SS0_B-TP1 | IO | QSPI B Slave Select 0; Active Low |
| 18 | BASE_PER_3V3-TP1 | P | Base board 3.3V |
| 19 | GND-TP1 | P | Digital Ground |

2.3.17 JTAG

The VAR-DT8MCustomBoard exports the DART-MX8M JTAG signals through a standard 1.27" 10 pin Header.

2.3.17.1 JTAG Header Pin-out (J29)

Table 2-27 JTAG Header Pin-out (J29)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---|
| 1 | JTAG_VREF | O | JTAG IO reference voltage. Connects to SOM_NVCC_3V3 - SOM peripherals 3.3V supply output. |
| 2 | JTAG_TMS | I | JTAG Mode Select signal |
| 3 | GND | P | Digital Ground |
| 4 | JTAG_TCK | I | JTAG Clock signal; Requires 10K pull down. |
| 5 | GND | P | Digital Ground |
| 6 | JTAG_TDO | O | JTAG Data Out signal |
| 7 | GND | P | Digital Ground |
| 8 | JTAG_TDI | I | JTAG Data In signal |
| 9 | JTAG_NTRST_C | I | JTAG Reset signal |
| 10 | NRST_CON | IO | Programmer Reset; Open Drain; Used to put the SOC in reset state. |

Note
J29 is not assembled.

2.4 User Interfaces

2.4.1 LED Indications

2.4.1.1 Power-On LEDs (D35, D34)

Two LED indicators used:

- **D35** indicates that the VAR-DT8MCustomBoard VCC_5V DC IN power after the over voltage and current limiter IC of is ON.
- **D34** indicated the SOM power is ON

2.4.1.2 GP LEDs (D7, D10, D12, D14)

LEDs **D7**, **D10**, **D12** and **D14** are General Purpose functionality LED controlled by DART-MX8M's GPIO.

NOTE

GPIOs controlling GP-LEDs are used by the DART-MX8M as the boot configuration. Care should be given not to drive them before rise of POR_B signal + 1ms.

2.4.2 Control Buttons

2.4.2.1 Boot Select (SW7)

The Boot select switch SW7 sets the DART-MX8M boot source & sequence. Refer to the DART-MX8M module data sheet for detailed Boot description.

Table 2-28 Boot Select modes (SW7)

| Position | Logic Level | Boot Source |
|----------|-------------|-----------------|
| ON | High | External (SD) |
| OFF | Low | Internal (eMMC) |

2.4.2.2 Power Switch (SW8)

The Power Switch SW8 Connect/Isolate the DC Power input at U31 TPS25942ARVCT output to the VAR-DT8MCustomBoard regulators.

U31 functions as a eFuse with multiple power protection modes.

Note

U31 is powered once a power source is available on J4 or J40, regardless of SW8 state!

2.4.2.3 User Buttons (SW1, SW2, SW3, SW4)

SW1, SW2, SW3 and SW4 are User Buttons connected to the DART-MX8M GPIOs for general purpose.

In Linux release they can be configured as e.g. Left, Enter, and Right Buttons in the DTS file.

NOTE

***GPIOs used for reading user buttons are boot configuration inputs of the DART-MX8M.
Care should be given not to drive them before rise of POR_B signal + 1ms.***

2.4.2.4 Reset Button (SW6)

A press on SW6 will perform a system hardware-reset resulting in a complete power cycle of the DART-MX8M.

2.4.2.5 ON/OFF Button (SW6)

The ON/OFF is Button supports the following:

1. **In OFF mode:** A brief button press causes the internal power management state machine to change state to ON.
2. **In ON mode:** A brief button press generates an interrupt (intended to initiate a software-controllable power-down).
An approximate 5 second or more button press causes a forced OFF.

2.4.3 Power

The VAR-DT8MCustomBoard is powered by a +5V power supply, connected either through a 2.0 mm power plug or alternatively through a 2 pin Terminal block.

A 5V fan power output is available via shrouded 2 pin header. Mating Housing Molex 22-01-3027; Connector Terminal Female Molex 08-50-0114;

2.4.3.1 DC-in Jack Pin-out (J4)

Table 2-29 DC-in Jack Pin-out (J4)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------|
| 1 | GND | P | Power supply return |
| 2 | GND | P | Power supply return |
| 3 | VCC_PJ | P | Power supply 5V |
| 4 | VCC_PJ | P | Power supply 5V |

2.4.3.2 DC-in Terminal Block Pin-out (J40)

Table 2-30 DC-in 2 pins Terminal Block Pin-out (J40)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|---------------------|
| 1 | GND | P | Power supply return |
| 2 | VCC_PJ | P | Power supply 5V |

2.4.3.3 DC-out FAN 5V Pin-out (J24)

Table 2-31 DC-out 5V FAN Header Pin-out (J24)

| Pin # | CustomBoard Signal | Type | Description |
|-------|--------------------|------|--|
| 1 | FAN_PWR | P | Power supply 5V out <i>Note: Power via Ferrite Bead</i> |
| 2 | GND | P | Ground Return |

Note
J24 is not assembled.

2.4.3.4 RTC Backup Battery (JBT1)

The VAR-DT8MCustomBoard features JBT1, a CR1225 battery holder for powering the On board ISL12057IUZ RTC Module.

3 Electrical Environmental Specifications

3.1 Absolute maximum electrical specifications

Table 3-1 DC Power Input absolute maximum electrical specifications

| | Min | Max |
|--------------------------|-------|-----|
| Main Power Supply, DC-IN | -0.3V | 6V |

3.2 Operational electrical specifications

Table 3-2 DC Power Input Operational electrical specifications

| | Min | Max |
|--------------------------|------|------|
| Main Power Supply, DC-IN | 3.5V | 5.3V |

Note

Values dictated by protection IC U31(TPS25942A) configuration.

4 Environmental specifications

Table 4-1 Environmental specifications

| | Min | Max |
|--|---------|-------|
| Commercial operating temperature range | 0°C | +70°C |
| MTBF | >10kHRS | |
| Relative humidity, Operational | 10% | 90% |
| Relative humidity, Storage | 5% | 95% |

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