**Revision History**

<table>
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<tr>
<th>Document</th>
<th>Carrier</th>
<th>Description</th>
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</table>
| 1.0       | 2.0     | Changes from DOC 1.9 Carrier 1.4D include:  
- Optimisation for DART-MX8MP:  
  - Added external ethernet PHY  
  - Control IOs used on previous version over SA11 now controlled via I2C expander  
  - Added DSI header option for DART-MX8MP stock item exposed pins; Pinout compatible to Symphony J7+J8  
  - Native USB ID usage added important note  
  - USB Type C active discharge replaced with bleeder  
  - USB Type C crossbar differential switch simplified.  
- Removed DT8M NAND option  
- Added QSPI header J41 - located in location of J25  
- J27 & J28 pinout aligned to Symphony  
- Added PD on J1.38 for BSP CustomV2.0 signal.  
- Added additional CAN PHY on MX8MP  
- U44 footprint modified from SOIC to DFN  
- SD card power switch modified  
- Main power switch type align to Symphony  
- DART-MX8M DP connector replaced with 40pin eDP REF. design  
- PINMUX page deleted - reference to XLS  
- Ared reference design for 12Mb/s CAN-FD transciever  
- Due to EOL:  
  - U60,U62 changed to NFL18ZT207H1A3D  
  - Due to Allocation Problems: U45,U59 changed to SN65HVD232QDR  
| 1.1       | 2.1     | * GPLED4 controlled via FET Q14 to support DART-MX8M-PLUS 1.8V voltage level  
- Updated GPIO expanders U56,U57 footprint  
- Added note for U53 recommended P/N  
| 1.2       | 3.0     | * Due to EOL:  
  - Changed BOM P/N: U23,U45,U46,U56,U59,U57  
  - Added optional resistors R291-R294  
  - Changed Assembly: U31 Not assembled, R167 assembled  
  - Changed Ethernet PHY to ADIN1300: Changed Ethernet2 schematics, Added R295  
  - Changed J5 P/N and schematics to support ADIN1300 PHYs  
  - Updated comments on schematic nets  
  - R94-R97, R114-R117 assembled with Ferrite Bead  
| 1.3       | 3.0A    | * Due to EOL:  
  - U60,U62 changed to NFL18ZT207H1A3D  
  - Due to Allocation Problems: U45,U59 changed to SN65HVD232QDR  

**Disclaimer:**

Schematics are for reference only. Variscite LTD provides no warranty for the use of these schematics. Schematics are subject to change without notice.
**VAR-DT8MCustomBoard V2.x**  

**DART-MX8M-PLUS**

- **Board to Board Connection**: X2 Serial Camera 4 lanes
- **USB Type Micro-AB**: USB to UART
- **FTDI Header**: UART1
- **Ext. Header**: UART2
- **I2C Cap. Touch**: I2C2
- **SPDIF**: I2C3/4/5/6
- **Ext. Header**: CAN PHY
- **Resistive Touch Controller**: CAN FD
- **Header**: SAI 1/2/5/6
- **I2C**: I2C1: Internal to SOM
- **GPIOx**: GPIO1, GPIO2, GPIOx
- **JTAG**: JTAG
- **USB Type-C**: USB Type-C OTG
- **CAN PHY**: CAN FD x1

**Important Notes:**
1. Length match for HS signals according to SOM DS
2. USB routed as 90 ohm Diff pairs
3. PCIe/SATA routed as 85 ohm Diff pairs
4. LVDS routed as 100 ohm Diff pairs
5. Other fast changing signals routed as 50 ohm
DART-MX8M-MINI Connectors

For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS" located at:

Note: Pinname with /*/ prefix denotes a HW assy option.
For complete alternate function per pin and specific SOM:
please refer to "DART_Compatibility_and_Pinout.XLS" located at:

Note: Pinname with /*/ prefix denotes a HW assy option.
Customboard 5V power supply is limited to 3A, shared with Board's USB devices. Do not connect devices which exceed current limitations.
11. BOOT CONFIG & MODE

Notes:
- Sampled on rising edge of POR_B
- SOC PD during POR_B and after
- BOOTMODE[1:0] = "10" is Internal Boot - Always used.
- Active boot cfg for one dip sw sel EXTERNAL/INTERNAL

DART-MX8M-MINI Notes:
- Boot config lines do not follow the Mini datasheet in full
- DART-MX8M-MINI have added logic to be compatible to DART-MX8M

DART-MX8M-PLUS Notes:
- Boot configuration set only by SAI1_TXD2 connected on DART via buffer to BOOT_MODE0

Notes:
- Tristate buffers required not to pull
- Buffers required for DART-MX8M & DART-MX8M-MINI
- For DART-MX8M-PLUS only U13 required

U17 U18 U19 Notes:
- Tristate buffers required not to pull
- Buffers required for DART-MX8M & DART-MX8M-MINI
- For DART-MX8M-PLUS only U13 required
13. CAN FD Interface

SPI based CAN-FD Controller 8Mb/s limited

CAN PHY
5Mb/s Limited

CAN PHY 12Mb/s Reference Design Only!

NOTE FOR U59A U45A
- Located on bottom side
- When assembling the ADM3058E IC removal of TCAN332 is a must!
13. **DART-MX8MP - ENET1 Gigabit Ethernet**

**Straps:**
- LEDs - active HIGH, address 00001b
- SOM PHY MDIO address 0000b

**Layout Notes:**
- Place 10nF & 100nF capacitors for each power pin.
- Place the capacitors as close as possible to the chip.

**NOTE:**
- For DT8MP net SOM VDD_PHY_1V8 connected to NVPCC_SAI1_SAI5 which is an output from the DT8MP programmable PMC LDO.
- This output voltage will set SAI1 and SAI5 pads voltage level.
- With DT8MCustomBoard V1.x and earlier it is set to 3.3V.
- On DT8MCustomBoard V2.x it is set to 1.8V for RGMII.
- Bypass with 4.7uF min. 6.3V capacitor.

**NOTE for uR3:**
- Required for compatibility to DT8M & DT8MM where SAI1 levels are fixed to 3.3V.

**NOTE:**
- Test points below used to access DT8M & DT8MM SAI1 signals.
- Levels are fixed to 3.3V by modules.

**Title Size Document Number Rev**

**Approved By:**
- Designer: Leonid S.
- Date: Monday, April 04, 2022