01. COVER

Disclaimer:
Schematics are for reference only.
Variscite LTD provides no warranty for the use of these schematics.
Schematics are subject to change without notice.

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Revision History

<table>
<thead>
<tr>
<th>Document</th>
<th>Carrier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Rev 1.2</td>
<td>Release</td>
</tr>
<tr>
<td>1.1</td>
<td>Rev 1.2</td>
<td>SAI1 &amp; SAI2 pin names switched to follow the SOM</td>
</tr>
<tr>
<td>1.2</td>
<td>Rev 1.2</td>
<td>CPI Pins added to extension headers</td>
</tr>
<tr>
<td>1.3</td>
<td>Rev 1.21</td>
<td>Removed I2C2 pull up resistors</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Removed not connected boot strap, uSD, Ethernet resistors</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added boot strap table</td>
</tr>
<tr>
<td>1.4</td>
<td>Rev 1.21</td>
<td>Changed J1.63 pin name</td>
</tr>
<tr>
<td>1.5</td>
<td>Rev 1.21A</td>
<td>32khz clock for Wi-Fi module is supplied from iMX6UL processor. R44 not connected, R45 connected</td>
</tr>
<tr>
<td>1.6</td>
<td>Rev 1.22</td>
<td>Added filtering on Audio Line In, Headphone lines</td>
</tr>
<tr>
<td>1.7</td>
<td>Rev 1.23</td>
<td>R105 pull-down and delay mechanism added on DEBUG_UART_RTS_B to allow reboot from SD Card using POR button</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Watchdog signal connected to POR circuitry for proper SW reset</td>
</tr>
<tr>
<td>1.8</td>
<td>Rev 1.23</td>
<td>Updated page 3 note 13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated page 7 On/Off signal note</td>
</tr>
<tr>
<td>1.9</td>
<td>Rev 1.23</td>
<td>Updated page 8 pinmux of pins J1.35, J1.43</td>
</tr>
<tr>
<td>2.0</td>
<td>Rev 1.23</td>
<td>J2.77, J2.83 - Added note for SOMs with iMX6UL ‘G3’ variant</td>
</tr>
<tr>
<td>2.1</td>
<td>Rev 1.23</td>
<td>Updated note for UART2 interface</td>
</tr>
<tr>
<td>2.2</td>
<td>Rev 1.23A</td>
<td>RI07 value changed to strong Pull Up to prevent system reset when entering suspend</td>
</tr>
<tr>
<td>2.3</td>
<td>Rev 1.23A</td>
<td>Added note for USB ports</td>
</tr>
<tr>
<td>2.4</td>
<td>Rev 1.23A</td>
<td>U11: PN text changed to KSZ8081RNBCA to align with the actual assembly</td>
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</table>
In SOMs assembled with iMX6UL 'G3' variant automatic SD1 routing selection is not available. In such SOMs, controlling SD1 interface routing should be done manually using pins J2.77 and J2.83 as follows:

- **J2.77**: Floating
- **J2.83**: Connect to 3.3V

**SD1 interface routed to WiFi**

- **J1 SD1 interface routed to WiFi**

Please see note for pins J2.77, J2.83 (13)

**Pull down resistor required for boot from SD-Card**

Please refer to note on page 6.

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**ETH1 Interface**

- **ETH1 Interface** is used by on SOM PHY.
- The lines should be not connected when the internal PHY is used. GPIO

**SAI1 Interface**

- **SAI1 Interface** is used only by on SOM with both BT Audio and AUDIO codec assembled

**I2C2 Interface**

- **I2C2 Interface** is used by on SOM Peripherals. The addresses in use by SOM are: 0x1A, 0x50, 0x51.

**OSC_32K_IN** is used on SOM WiFi module. Usually this pin is connected to J2.28

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**Title Size**

- **Document Number**
- **Rev**

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**Note:**

- In SOMs assembled with Linux 'G3' variant automatic SD1 routing selection is not available. In such SOMs, controlling SD1 interface routing should be done manually using pins J2.77 and J2.83 as follows:
- **J2.77**: Floating
- **J2.83**: Connect to 3.3V

Please see note for pins J2.77, J2.83 (13)

**Pull down resistor required for boot from SD-Card**

Please refer to note on page 6.

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**Variscite**

- **Project**
- **Date:** 3 Sep 2017
- **Project:**
- **Date:** Sheet 1.23
06. SD, USB

Note: Pull down resistor and delay circuitry is added on DEBUG_UART_RTS_B to allow reboot from SD Card using POR signal, since USB_OTG_ID is not connected - USB role Host/Device is determined in SW.

Note: USB Debug UART RTS pin is not connected - USB role Host/Device is determined in SW.
The On/Off button is connected to the On/Off signal of the iMX6UL CPU. Long press (approx 7 sec) on this button will reset the module. In order to achieve this: assemble R62, R46; disassemble R47 and R69; insert the coin cell battery into JBT1.